D2.3 – Architecture design for converter applications

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DISCLAIMER

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PROJECT SUMMARY

SiC4GRID is a 42-month project gathering partners from the complete value chain of SiC-based converters collaborating to tackle current obstacles to the technologies' market uptake. SiC4GRID thus aims for an optimised integrated SiC-based technology composed of three-fold innovations in terms of hardware, software and IoT.

To optimise both techno-economic and environmental pillars, the consortium will design, produce, test and validate an integrated product composed of a 30% smaller size energy-efficient SiC-based power module competitive with state-of-the-art technology and coupled with an adapted optimised self-healing energy management system (EMS). This EMS amplifies the benefits of a strong system-level IoT architecture and adapted digital tools such as digital twin and optimisation algorithms.

Throughout the project, the circularity and eco-design of all steps of the converter manufacturing process will be targeted with a strong emphasis on resource optimisation and carbon emission reduction. The testing phase will be done both as an integrated modular converter on a physical test bench, as well as digitally to increase the variety of relevant applications and real-condition scenario. For the digital simulations, three use cases will therefore be chosen to increase the validated parameters and scope of applications, including MMC and SST converters, onshore/offshore wind and PV applications, as well as the potential for storage.

Overall, the project contributes to advancing the market readiness of the technology by lowering its cost (30% cost reduction compared to silicon converters), its size (15% size reduction), its lifetime (30+ years) and its environmental impact (30% resource consumption reduction and 50% CO2 emission reduction). In the longer-term, SiC4GRID will thus also help renewable energies integrate the energy grid and bring European leadership to the forefront of converter technology providers.

OBJECTIVE AND EXECUTIVE SUMMARY

This document is a report on the design optimisation and performance evaluation of selected PE system architecture for defined converter applications.

The objective of this report is to describe the design optimisation of the system architecture for the three use case scenarios described in Deliverable 1.2. The architecture is considered in terms of power electronics converters topologies, modularity and ratings, with the SiC-based modules developed in WP3. The objective is to optimise the architecture in terms of cost, efficiency and lifetime.

The first part of the report describes the optimisation framework developed in T2.1 “Co-design optimisation of the SiC power modules for converter applications towards longer lifetime and lower cost”, suited to the three project use case scenarios.

The second part of the report describes the modelling of the SiC power modules performed in T2.2 “Low- to medium-fidelity modelling of SiC power modules”, which is used in the design optimisation framework the replicate the behaviour of the actual system.

Finally, based on the use case definitions, the optimisation framework and the modelling, the optimisation results are presented with relevant sensitivity analysis. This provides a clear evaluation of the proposed topologies and optimised architectures towards lower cost, higher efficiency and longer lifetime.

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ABBREVIATIONS AND ACRONYMS

Table 1: List of Acronyms

Acronym	Description
AC	Alternating Current
CAPEX	Capital Expenditure
CINEA	European Climate, Infrastructure and Environment Executive Agency
D4HR	Design for High Reliability
DAB	Dual Active Bridge
DC	Direct Current
EMS	Energy Management System
GA	Genera Assembly
HOF	Holistic Optimisation Framework
IoT	Internet of Things
KPI	Key Performance Indicator
MF	Medium Frequency
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
NSGAII	Non-Dominating Sorting Genetic Algorithm II
OPEX	Operational Expenditure
PE	Power Electronic
PSD	Power Semiconductor Device
PU	Per Unit
PV	Photo Voltaic
Si	Silicon
SiC	Silicon Carbide
SM	Submodule
SST	Solid State Transformer
TCO	Total Cost of Ownership
UC	Use Case
WP	Work Package

Table 2 - Partners Acronyms

No.	Participant name	Acronym	Country
1	VRIJE UNIVERSITEIT BRUSSEL	VUB	BE
2	AALBORG UNIVERSITET	AAU	DK
3	ELECTRICITE DE FRANCE	EDF	FR
4	SOITEC AS	SOITEC	FR
5	POWERCON AS	PWC	DK

6	KK WIND SOLUTIONS AS	KKW	DK
7	INFORMATION TECHNOLOGY FOR MARKET LEADERSHIP	ITML	EL
8	MONDRAGON GOI ESKOLA POLITEKNIKOA JOSE MARIA ARIZMENDIARRIETA S COOP	MGEP	ES
9	EUROQUALITY SARL	EQY	FR
10	HITACHI ABB POWER GRIDS LTD.	HE	CH
11	CSEM CENTRE SUISSE D'ELECTRONIQUE ET DE MICROTECHNIQUE SA - RECHERCHE ET DEVELOPPEMENT	CSEM	CH
12	AMANTYS POWER ELECTRONICS LTD	AMTS	UK

1 INTRODUCTION

The SiC4GRID project aims for an optimised integrated SiC-based technology composed of three-fold innovations in terms of hardware, software and IoT. In Task 2.1, VUB is responsible for developing a holistic design optimisation framework (HOF) that will consider the different project KPIs as multi-objective functions to find the right sizing of components inside the system with Design for high reliability (D4HR) approach to achieve higher efficiency, longer lifetime and lower cost.

As part of the SiC4GRID optimisation framework, three objective functions have been considered (a) converter efficiency over the entire profile, (b) total cost of owning comprising capital expenditure (CAPEX) and operational expenditure (OPEX) and (c) overall system reliability. The framework also considers the relevant data of the innovative high-voltage SiC LinPak device from Hitachi Energy and different power electronics converter topologies (e.g., half-bridge, 1-phase dual active bridge, 3-phase dual active bridge) with actual load profiles and system energy management strategy. This deliverable is an output of T2.1 and T2.2 and presents the results and analysis based on a stepwise HOF aimed at optimal selection and sizing of the most suitable power electronics interface for three different use cases. These use cases have been finalized as part of WP1 (see D1.2). The developed HOF is a modular and adaptable framework and has the merit of being utilized in various applications.

In the SiC4GRID project, a generic architecture has been employed for all three use cases, whereas only the models are exchanged. The developed HOF has dependency on several tasks: (a) the system architecture (e.g., in PV UC, total no of PV farm and their topology) and specifications defined in WP1; (b) design variables defined as per project GA; (c) SiC LinPak characteristics based on T3.2 data; (d) PV, wind and load profile defined by project partner EDF as part of WP1 and (d) cost indicator for different bill of materials defined based on the discussion with different project partners, especially PWC, KKW, EDF and AAU. The input/output interaction of T2.1 with other tasks is summarized in Figure 1.

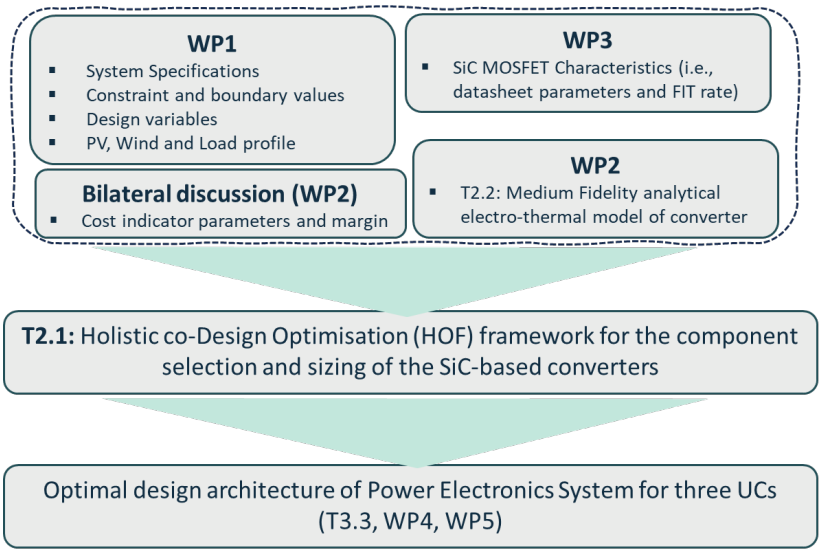


Figure 1: Input/output interaction between Task 2.1 and other WPs (i.e., WP1, WP3, WP4 and WP5) throughout the SiC4Grid project.

To oversee the complete development of the framework, we have employed the classical V-design cycle, as illustrated in Figure 2. The figure demonstrates the various stages of the framework's development. The initial phase involves defining the framework, which encompasses tasks such as identifying requirements, developing the framework for the photovoltaic (PV) use case, modelling the PV use case using initial models, and adapting the framework for the wind use case.

The completion of the definition phase sets the stage for the subsequent implementation phase. This phase involves seamlessly integrating the comprehensive analytical model into the overarching framework. It includes the generation of results for individual use cases (UCs) and finishes after completing the comparison and evaluation of these results in relation to the targeted Key Performance Indicators (KPIs) of the SiC4GRID project.

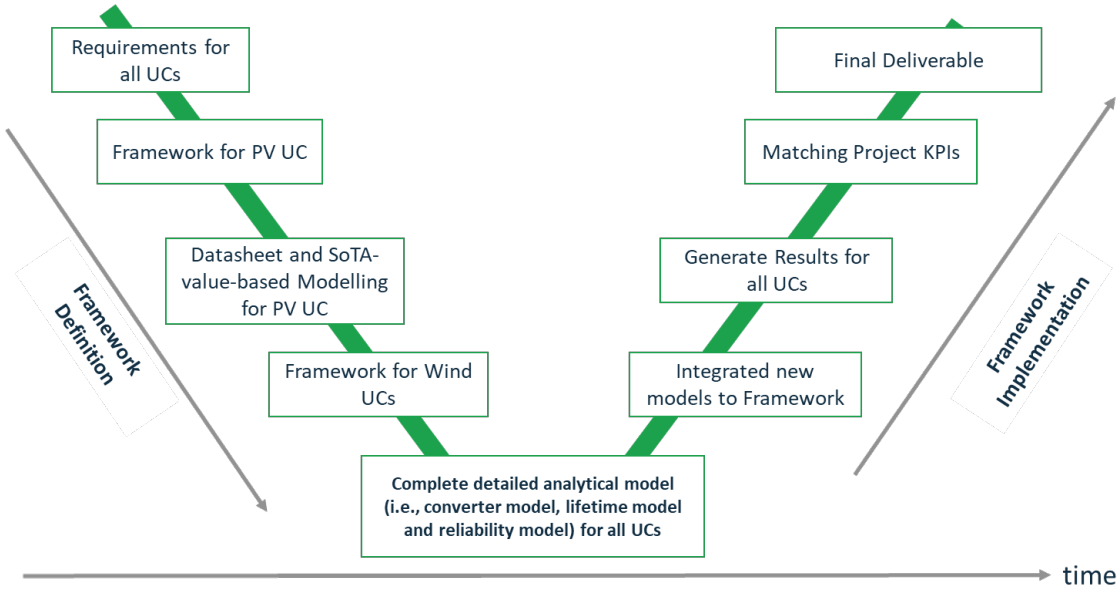


Figure 2: V-cycle approach to follow up the development and implementation of the HOF framework.

2 GENERIC HOLISTIC OPTIMISATION FRAMEWORK

2.1 SPECIFICATIONS OF THE SIC4GRID USE CASE SCENARIOS

This section provides a summary of the three use cases employed in the project. The details of the use cases were provided in D1.2.

2.1.1 First Use Case: PV-SST Use Case

The first use case of the project considers a PV farm. The purpose of this use case is to determine the optimum architecture for a DC/DC SST converter.

The structure of the PV farm comprises of numerous PV panels. Several PV panels are connected in series to form a low-voltage DC bus. In order to transfer electrical energy, this low voltage level should be increased. Low voltage to medium voltage energy conversion is performed by the modular multilevel DC/DC SST. After the energy transfer, a medium voltage DC to AC inverter is utilized in order to connect the PV farm to the transmission system.

Many submodules are utilized to form the modular multilevel DC/DC SST. Every submodule of the SST consists of a medium frequency transformer, power switches, and capacitors. Depending on the implemented topology, the number of power switches and capacitors may change.

At the input side, submodules are connected electrically in parallel to have high current and low voltage operation. At the output side, submodules are connected in series to obtain the low current and high voltage operation. The number of submodules of the converter depends on the output voltage.

Four SSTs are connected electrically in parallel to form a 10 MW building block for the PV farm. These building blocks are the fundamental units used in the design of the PV farm. Two building blocks are connected to form an array. Arrays are connected in parallel electrically and positioned in a vertical column. Three of these arrays are connected to the same DC bus collector. Four of these structures are connected to have the total PV farm, resulting in a total power of 240 MW for the farm.

The overall structure of the SST and the PV farm is illustrated in Figure 3 and the specifications of the PV farm are listed in Table 3.

Table 3: PV-SST Use Case Specifications.

Description	***Value***
PV panel rated power	615 W
Total no of PV panel in a string	27
Total no of string	150
Total rated power of PV farm	240 MW
Power rating of a single DC/DC SST converter	2.5 MW
Power rating of a building block (bb)	10 MW
Input voltage of the SST DC/DC converter	1.5 kV
Targeted output voltage	5 kV-60 kV

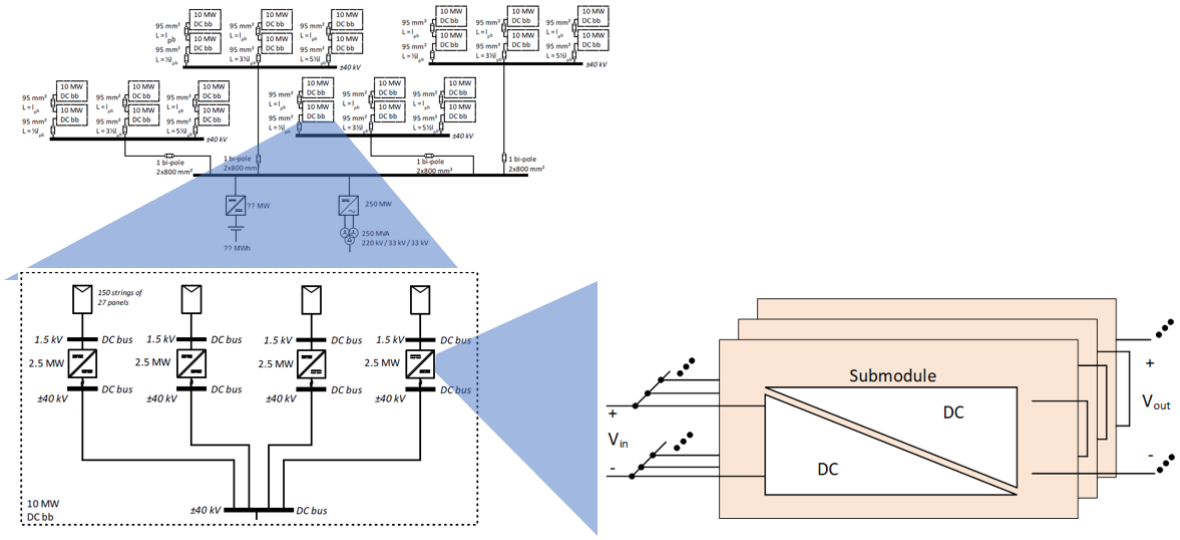


Figure 3: Block Diagram of the PV-SST Use Case Showing Detailed Structure of a 10 MW DC/DC Building Block and DC/DC SST Submodule Structure

It should be noted that in order to achieve maximum power point tracking (MPPT), an independent DC/DC converter should be connected to every string of the PV panels. This DC/DC converter should have 17 kW rated power. The design of these converters is out of scope of this use case.

For the optimisation of the use case, a changing PV farm power profile for one year is considered. This power profile is provided by a project partner and shown in Figure 4.

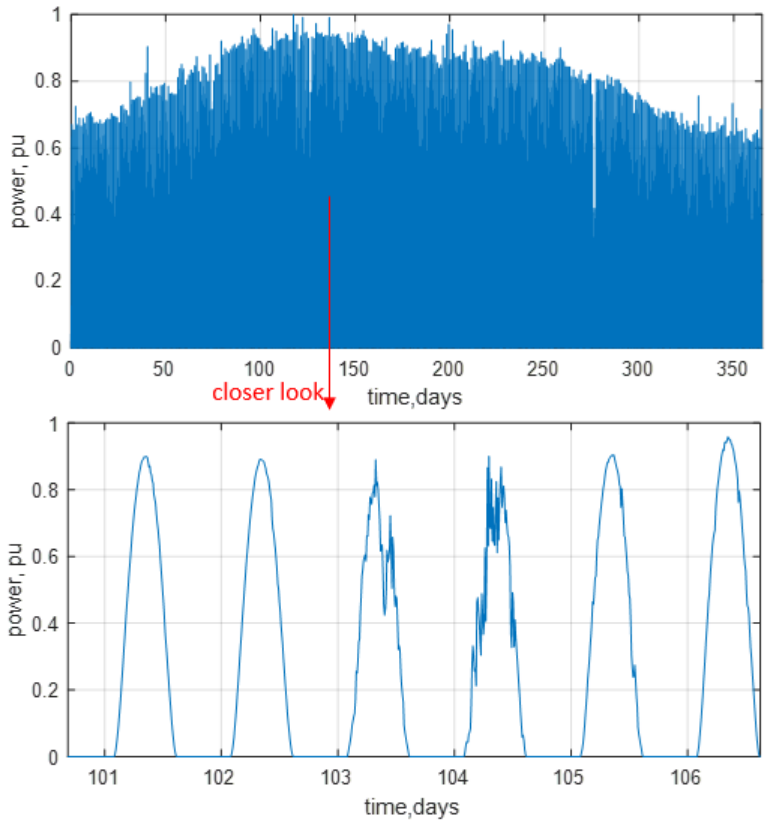


Figure 4: PV Farm Power Profile

2.1.2 Second Use Case: Wind-MMC Use Case

In this use case, the energy conversion unit of a single offshore wind turbine is analysed. The wind turbine generator has varying frequency and varying amplitude AC output. In order to utilize the electrical energy generated by the wind turbine in the electricity grid, its amplitude and frequency should be fixed. For this purpose, a medium frequency AC/AC converter is required. A back-to-back AC/AC MMC is designed to fulfil this requirement.

The MMC is mainly implemented with inductors, power switches and capacitors. The unit structure of the MMC is a cell. The cells are connected in series to form an arm structure. Six symmetric arms are used to form one half of the back-to-back converter. DC sides of two halves are combined to form the complete MMC. Figure 5 shows the structure of the MMC system and the specifications of the use case are listed in Table 4.

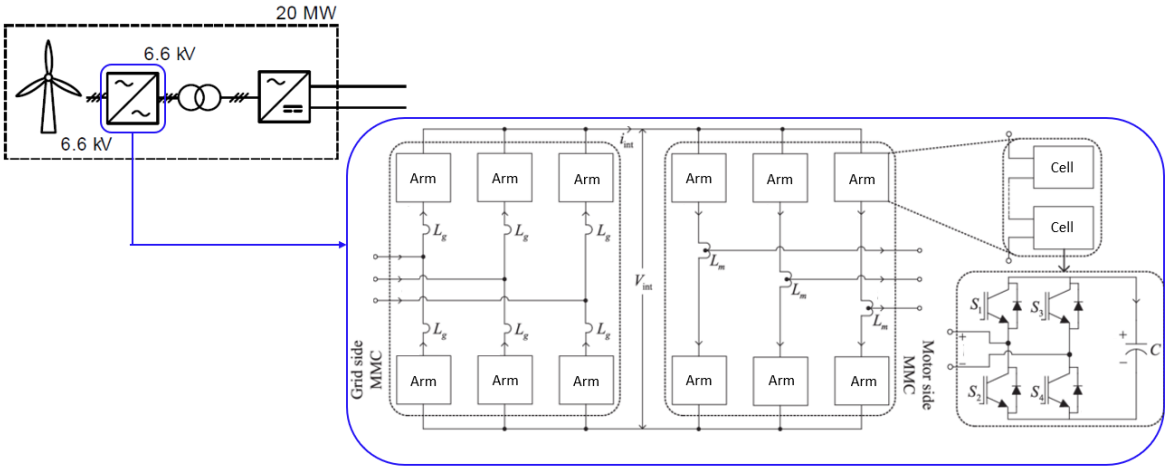


Figure 5: Wind-MMC Use Case System Diagram [1]

Table 4: Wind-MMC Use Case Specifications.

Description	***Value***
Power rating of the wind farm	20 MW
Generator voltage	6.6 kV
Line voltage	6.6 kV
Line frequency	50 Hz

A varying wind power profile is applied to run the optimisation framework. The power profile is a 24-hour profile provided by a project partner. The power profile is shown in Figure 6.

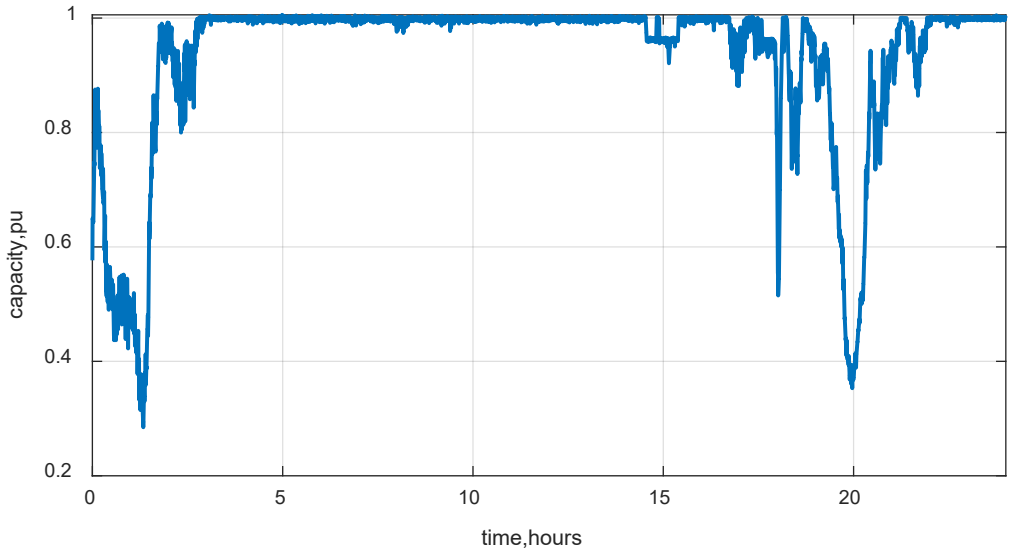


Figure 6: Wind Farm Power Profile

2.1.3 Third Use Case: Wind-SST Use Case

An offshore wind farm case is considered in the final use case. Unlike the second use case, DC transmission is utilized in the third use case. Therefore, after turning the AC voltage of the wind turbine generator to DC voltage, a DC/DC step up converter is necessary to increase the voltage level. Similarly to the first use case, a modular multilevel DC/DC SST converter is implemented to fulfil this requirement.

The input voltage level of the SST is significantly higher than the first use case. Therefore, submodules are connected both in parallel and in series at the input side of the SST. The structure of the converter is illustrated in Figure 7.

Since the SST is connected to DC transmission cables directly, the cable size is a design parameter for this use case. Therefore, instead of considering a single wind turbine, a wind turbine farm is considered in this use case. The specifications of the use case are listed in Table 5.

Table 5: Wind-SST Use Case Specifications.

Description	***Value***
Total no of wind turbines	15
Power rating of each wind turbine	20 MW
Total rated power of wind farm	300 MW
Distance of the farm from shore (Exporter cable length)	50 km
Distance between individual wind turbines	2.5 km
Input voltage of the SST converter	8-10 kV
Allowable medium voltage level*	50-240 kV

*Since this voltage is implemented in the nacelle, in the implementation stage the voltage will be limited to lower values due to insulation requirements. Provided numbers are used for research purposes.

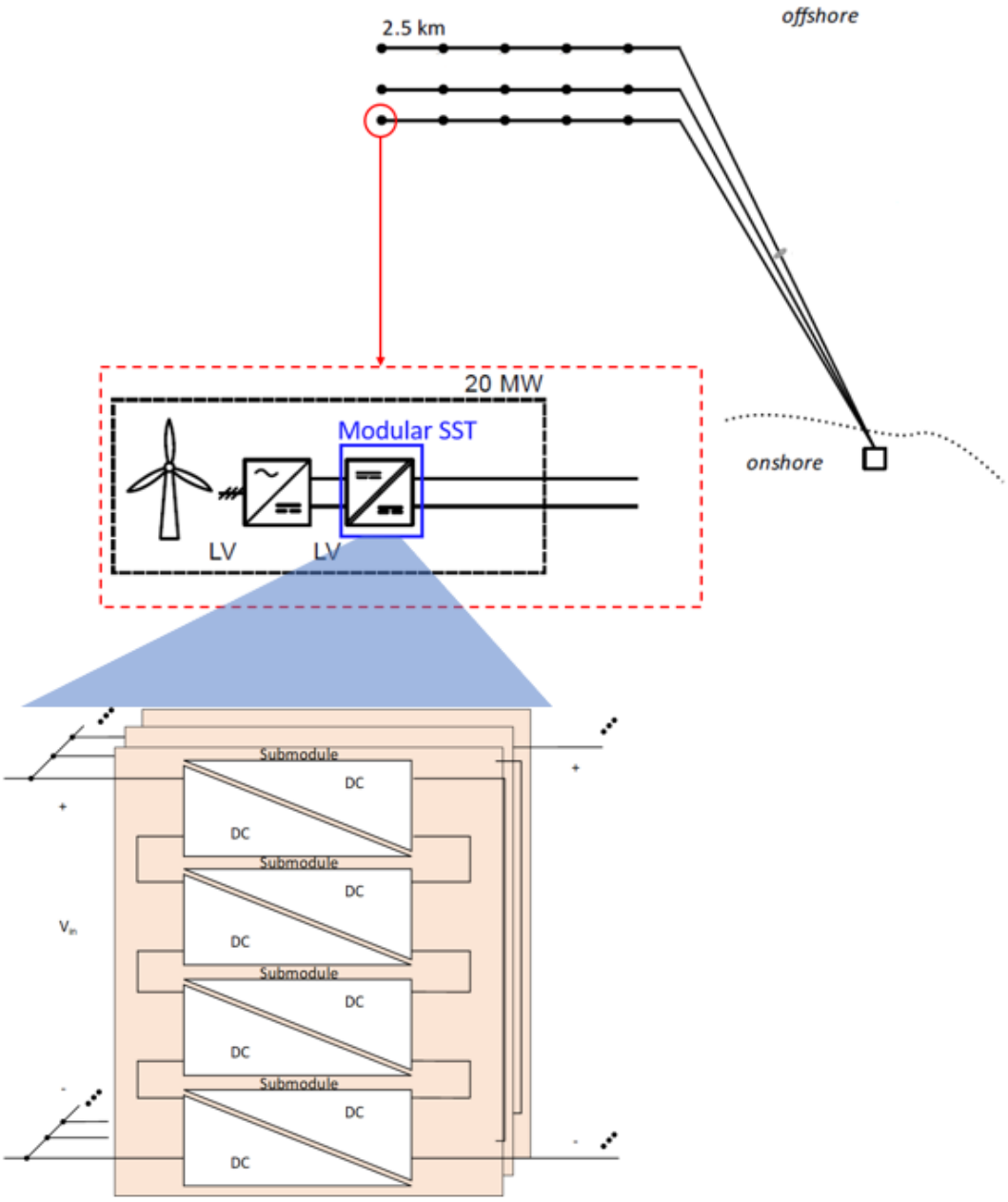


Figure 7: Offshore Wind Farm and Multilevel Modular DC/DC SST Structure

2.2 DESCRIPTION OF THE HOLISTIC OPTIMISATION FRAMEWORK

The purpose of this framework is to optimise the efficiency, lifetime, and cost of MMCs and SSTs for two selected renewable energy applications. The procedure begins by obtaining the use case specifications. Next, the required SiC-based switch information is retrieved from the SiC device database. Submodules of the converters can have different topologies, and information about alternative submodule topologies is added in this step. In the subsequent phase, converter behaviour is simulated to calculate efficiency, lifetime, and cost.

Using the simulation results, a non-dominated sorting genetic algorithm (NSGAII) determines the Pareto solution set for the use case. The algorithm initiates by creating a population of random

variables according to the constraints of the use cases. Then, using the initial population, a child population is formed by using operators of mutation and crossover. The child population and the previous generation are merged to reach the next generation. This process is repeated until the stop criteria is reached. At the end of the procedure, a non-dominating population or a Pareto solution set is obtained. This implies that within the final set, every solution is an optimal solution. In other words, none of the objective functions of a solution can be improved without degrading at least one other objective function.

Finally, from the Pareto solution set, an optimal solution is determined by a pre-determined weight function. Figure 8 shows the structure of the framework.

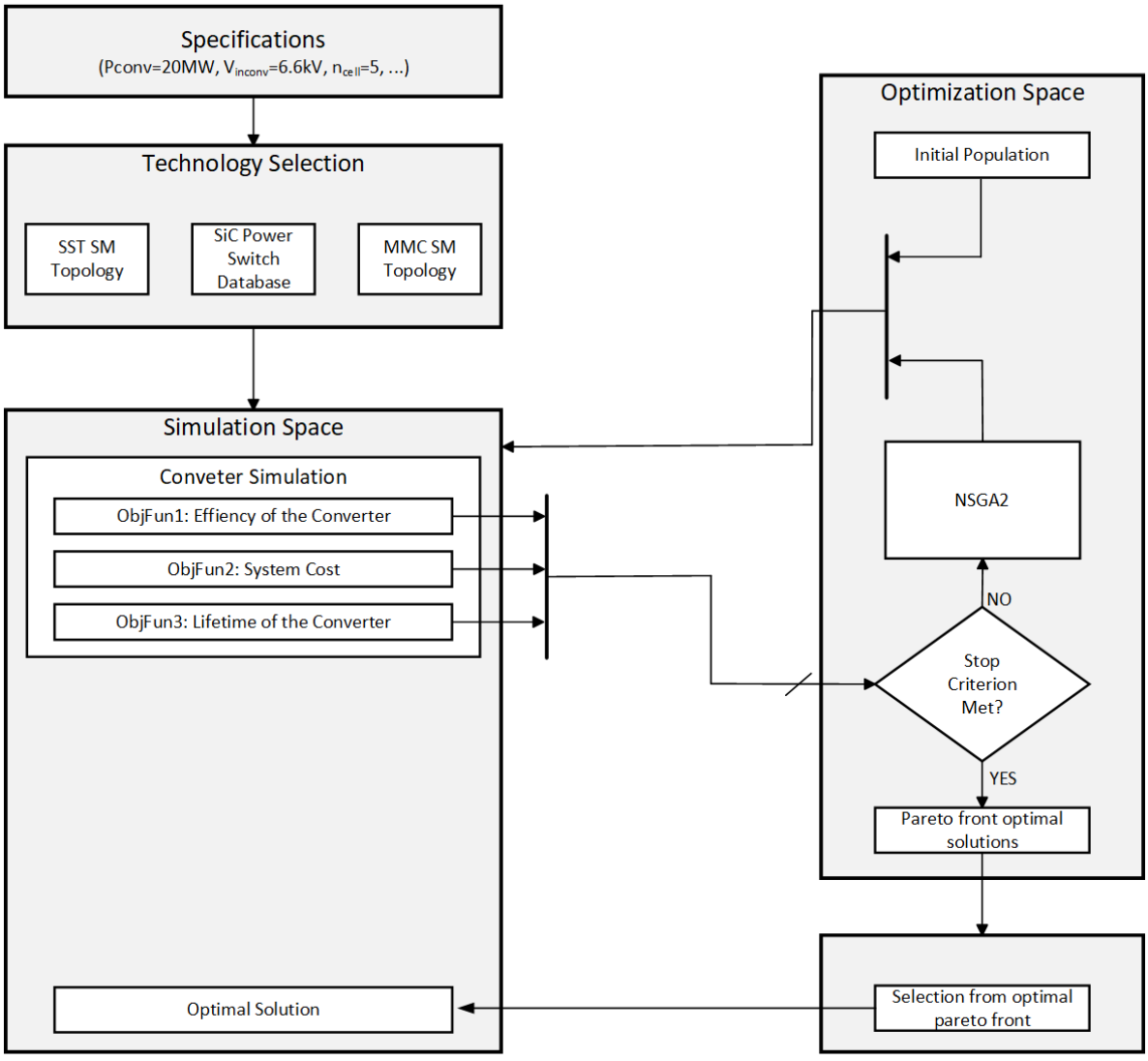


Figure 8: Stepwise Methodology of the Holistic Design Optimisation Framework.

2.2.1 Problem formulation

A generic multi-objective problem definition is used for the framework. The definition is shown below.

$$\begin{gathered} Minimize\ F(x) = [f_1(x), f_2(x), f_3(x)] \\ Subject\ to: g_i(x) \leq 0 \\ X = \{x \mid g_m(x) \leq 0, m = 1,2,3, \dots M\} \\ S = \{F(x \mid x\ \epsilon\ X)\} \end{gathered} \tag{1}$$

In this formulation, x is the vector of design variables, the inequality constraints vector is denoted with $g_i(x)$, the feasible decision space is denoted with X and m shows the number of inequality constraints. Finally, the criterion space is denoted with S. Different objective functions f_1, f_2 or f_3 are either minimized or maximized depending on the objective function. The optimisation in this deliverable is a discrete integer problem which means there is a finite number of values that can be used in the elements of vector x.

2.2.2 Objective function

In this optimisation framework, the goal is to have power electronics systems with high efficiency, low cost and high lifetime. Therefore, there are three objective functions used in the optimisation.

Efficiency objective function determines the average efficiency of the SiC based energy converters on a given operation profile. In order to determine the total energy loss, elements of the power loss are summed and then divided to the total energy input. Four main sources of energy loss are the conduction losses, switching losses, transformer losses and inductor losses. Details of the energy loss calculation are provided in the following sections.

The second objective function is the capital expenditure (CAPEX) of the system. CAPEX includes the CAPEX of the converter and the CAPEX of the system cable. These two parts of the system are included in the optimisation because they represent the difference between the traditional system and the systems with SiC based converters. Details of how to determine the CAPEX are given in the following sections.

The last objective function is the lifetime of the converter. The lifetime is defined as the time period for which the converter works with 90% probability. The reliability of switches is heavily effective on the lifetime of the converter. Moreover, converters regarded in this project are modular and have many submodules; therefore, lifetime and reliability are critical factors for the design.

2.2.3 Constraints and Specifications

The optimisation framework uses different constraints and specifications for each use case. These constraints and specifications are listed in Table 6, Table 7 and Table 8 for PV-SST, Wind-MMC and Wind-SST use cases respectively.

Table 6: Constraints and Specifications of PV-SST Use Case

Constraints/variables	Description	Specifications
$5\ kV \leq V_{metrans} \leq 60\ kV$	Medium voltage power transmission voltage	• Power level of the solar SST converter: 2.5 MW • Exporter cable length: 1km • Total number of converters: 96
$idx_{smtpo} \in [1,2,3]$	3 variants of DC/DC submodule topologies	
$1.8\ kV \leq V_{sw} \leq 2.2\ kV$	Maximum SiC based power electronics device voltage	
$0 \leq n_{rsm} \leq 2$	No of redundant submodules	
$12\ kHz < f_{sw} < 18\ kHz$	Switching frequency of the SST converter	
$1 \leq n_{para-swi} \leq 3$	No of parallel switches used in the converters	

Table 7: Constraints and Specifications of Wind-MMC Use Case

Constraints/variables	Description	Specifications
$12\ kV \leq V_{DC-link} \leq 26k\ V$	DC-link voltage of the MMC	• Power level of the wind turbine 20MW • Line voltage and generator voltage are 6600V_{rms} • Line frequency is 50 Hz
$7 \leq n_{cell} \leq 14$	Cell number of one upper arm of the MMC converter	
$f_{sw} = 800\ Hz$	Switching frequency of the converter	
$1 \leq n_{para-swi} \leq 3$	Number of parallel connected switches	
$idx_{smtpo} \in [1,2]$	Index for cell topology: 1=half bridge topology, 2=full bridge topology	
$1 \leq n_{rcell} \leq 3$	Redundant cell number	

Table 8: Constraints and Specifications of Wind-SST Use Case

Constraints/variables	Description	Specifications
$50\ kV \leq V_{metrans} \leq 240\ kV$	Medium voltage power transmission voltage*	• Power level of the wind turbine 20MW • Exporter cable length: 50km • Total number of converters: 15 • Distance between the turbines: 2.5km
$idx_{smtpo} \in [1,2,3]$	3 variants of DC/DC submodule topologies	
$1.8\ kV \leq V_{sw} \leq 2.2\ kV$	Maximum SiC based power electronics device voltage	
$0 \leq n_{rsm} \leq 2$	No of redundant submodules	
$12\ kHz < f_{sw} < 18\ kHz$	Switching frequency of the SST converter	
$1 \leq n_{para-swi} \leq 3$	No of parallel switches used in the converters	

*Since this voltage is implemented in the nacelle, in the implementation stage the voltage will be limited to lower values due to insulation requirements. Provided numbers are used for research purposes.

2.2.4 Optimiser Selection

The optimiser is designed to attain a Pareto solution set where each element within the set is optimised. In this context, no improvement can be made to any of the objective functions for an element without negatively impacting another. The NSGA II is utilized for generating the Pareto solution set. The specific settings for the optimiser are outlined below. Notice that MMC and SST use cases have different optimisation parameters. This is due to the difference between simulation ranges and simulation speeds of SST and MMC use cases.

PV-SST Use Case

- Population size: 1000
- Number of generations: 10
- Stall generation limit: 5

Wind-MMC Use Case

- Population size: 50
- Number of generations: 5
- Stall generation limit: 5

Wind-SST Use Case

- Population size: 1000
- Number of generations: 10
- Stall generation limit: 5

3 SIMULATION ENVIRONMENT: ANALYTICAL MODELLING

The optimisation framework includes simulation models for the converters used in the use cases. Depending on the use case, the model determines the power losses, cost and lifetime of the system. Hence, the model includes four main functions to determine these outputs.

In the following section, details of the simulation model and its functions are introduced.

3.1 ELECTRO-THERMAL MODELLING

3.1.1 Overview of DAB converters

Dual-active-bridge (DAB) converters are applied as submodules of the SST, due to the advantages of high-power density, inherent soft-switching capability, high efficiency, and galvanic isolation [2]-[3]. In this project, three topologies of DAB converters are considered, i.e., half-bridge DAB, single-phase full-bridge DAB, and three-phase DAB, as shown in Figure 9. Phase-shift control is the most popular control approach for the DAB converters, where the phase-shift angles and/or duty cycles are applied as control variables to regulate the power flow, and improve the performance of DAB converters, e.g., efficiency. For the half-bridge DAB converter, there is only one phase-shift angle between the two side bridges. As for the single-phase and three-phase DAB converters, various combinations of the phase-shift angles and duty cycles can be used for a certain transferred power. Therefore, optimal control strategies based on certain optimisation objectives (e.g., root-mean-square (RMS) current, and soft-switching operation) are widely discussed. In order to improve the efficiency of the single-phase and three-phase DAB converters by control strategies, multi-phase-shift control methods proposed in [4] and [5] are employed in this project, which can extend the ZVS range and also reduce the conduction losses by reducing the current stress.

Using the above control strategies, power loss modelling of the three DAB converters is carried out on a MATLAB code, which provides the basis for optimising between efficiency, reliability, and cost analysis. The power losses of the DAB converters can be mainly divided into the power losses of MOSFETs and power losses of magnetics, which are elaborated below.

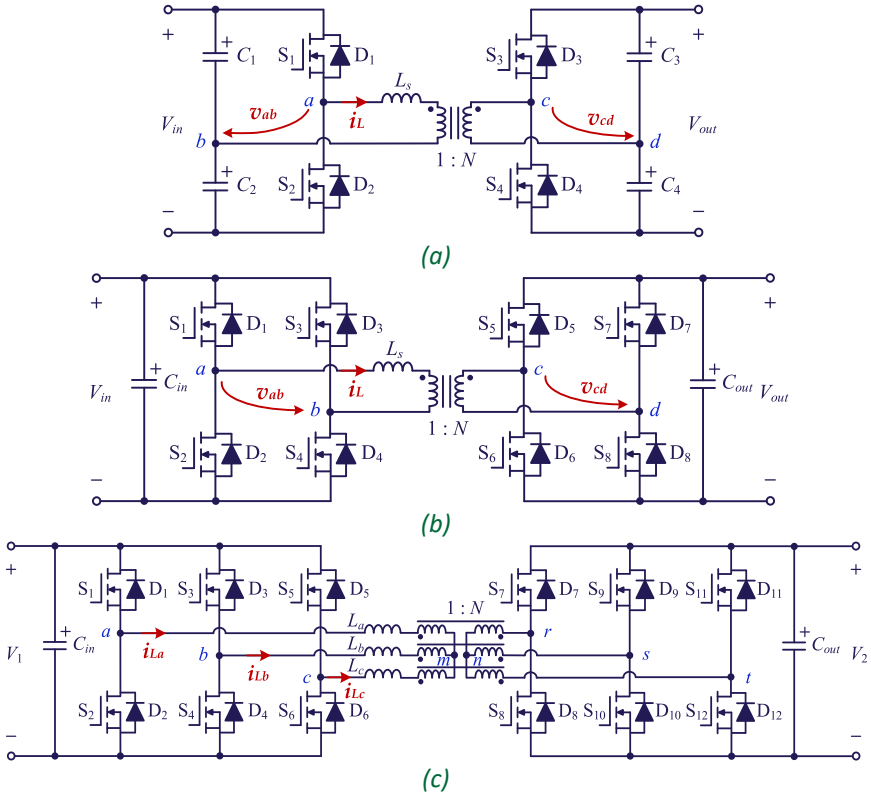


Figure 9: DAB converters with: (a) half-bridge, (b) single-phase, and (c) three-phase topology.

3.1.1.1 Electrical losses modelling

1) Conduction losses of MOSFETs:

The conduction losses for MOSFETs can be obtained by Eq. (2)

$$P_{CM} = R_{DSon}(T_j) I_{Drms}^2 \tag{2}$$

where $R_{DSon}(T_j)$ is the on-state resistance, and I_{Drms} is the root-mean-square (RMS) value of the inductor current. The on-state resistance is affected by the junction temperature, and expressed as

$$R_{DSon}(T_j) = R_{DSmax(25^\circ)}\left(1 + \frac{\alpha}{100}\right)^{T_j - 25^\circ} \tag{3}$$

2) Switching losses of MOSFETs:

The switching losses of MOSFETs are affected by the instantaneous voltage V_{dd}, current I_{ds}, and junction temperature T_j at the turn-on and turn-off instants, i.e.,

$$P_{SM\_on/off} = E_{on/off}(V_{dd}, I_{ds}, T_j) f_{sw} \tag{4}$$

The data of the switching losses E_{on} and E_{off} with respect to V_{dd}, I_{ds}, and T_j are provided by datasheet of the MOSFET. Thus, an Excel-based look-up table is made for the data of E_{on} and E_{off}, which is imported to the MATLAB code to calculate the switching losses of the MOSFETs.

3) Core losses of Magnetics

An isolated transformer and an auxiliary inductor (note: when the inductance is small, the leakage inductance can be used) are employed in the DAB converters to realize power transfer. Since the waveforms of the voltages and current are not sinusoidal, the Steinmetz equation is not suitable for

the core loss calculation. Instead, an improved Generalized Steinmetz equation (iGSE) model is used Eq. (5)-(6), i.e.,

$$P_{core\_Tr/Ls} = V_{Tr/Ls} f_{sw} \int_0^{T_{sw}} C_{m1} \left|\frac{dB(t)}{dt}\right|^{\alpha} |2\hat{B}|^{\beta-\alpha} dt \tag{5}$$

$$C_{m1} = \frac{C_m}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \tag{6}$$

where, C_m, α, and β are the coefficients of core material, $\hat{B}$ is the peak value of the flux density, and $V_{Tr/Ls}$ is the volume of the transformer/inductor. The flux density can be expressed as

$$\frac{dB(t)}{dt} = \frac{v_{Lm/Ls}(t)}{N_{Tr/Ls} A_{Tr/Ls}} \tag{7}$$

where, $N_{Tr/Ls}$ is the primary-side winding turns of the transformer/inductor, $A_{Tr/Ls}$ is the effective magnetic cross section of the transformer/inductor, and $v_{Lm/Ls}$ is the voltage across the magnetic inductance of transformer/inductor. Based on the equivalent circuit of the transformer and inductor, as shown in Figure 10, the voltage v_{Lm} and V_{Ls} can be obtained as Eq. (9)

$$v_{Lm}(t) = \frac{L'_{\delta 2}}{L_s + L_{\delta 1} + L'_{\delta 2}} v_{ab}(t) + \frac{L_s + L_{\delta 1}}{L_s + L_{\delta 1} + L'_{\delta 2}} \frac{v_{cd}(t)}{N} \tag{8}$$

$$v_{Ls}(t) = \frac{L_s}{L_s + L_{\delta 1} + L'_{\delta 2}} \left(v_{ab}(t) - \frac{v_{cd}(t)}{N}\right) \tag{9}$$

where, $L_{\delta 1}$ and $L'_{\delta 2}$ are the primary and secondary-side leakage inductance converted to the primary side.

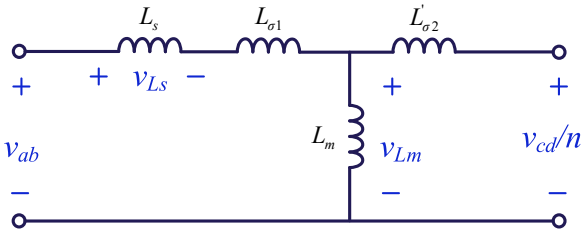


Figure 10: Equivalent circuit of transformer and inductor in DAB converters.

4) Copper losses of magnetics

The copper losses of the transformer can be obtained by

$$P_{copper\_Tr} = R_p I_p^2 + R_s I_s^2 \tag{10}$$

where, R_p and R_s are the resistance of the primary and secondary-side windings, respectively, and I_p and I_s are the RMS values of the primary and secondary-side currents. As for the auxiliary inductor, the copper losses can be calculated by

$$P_{copper\_Ls} = R_{Ls} I_p^2 \tag{11}$$

where, R_{Ls} is the resistance of the inductor windings. When ignoring some small losses, e.g., capacitor losses, the total power losses of the DAB converters can be obtained by

$$P_{DAB} = P_{CM} + P_{SM} + P_{core\_Tr} + P_{copper\_Ls} + P_{core\_Ls} + P_{copper\_Ls} \tag{12}$$

3.1.1.2 Thermal modelling

The junction temperature of MOSFET is determined by the thermal equivalent model, as shown in Figure 8, where R_{MOS}, R_{Gre}, and R_{HS} are the thermal resistances of the MOSFET module, thermal

grease, and heatsink, respectively. In Figure 11, *n* switches are placed on the same heatsink, and thus, the case temperature T_c at the heatsink surface can be calculated by

$$T_c = T_a + R_{HS}\sum_{i=1}^{n} P_{Loss\_Si} \tag{13}$$

and the junction temperature T_j for the i^{th} MOSFET can be obtained by

$$T_j(\mathrm{S}_i) = T_c + (R_{MOS} + R_{Gre})P_{Loss\_Si} \tag{14}$$

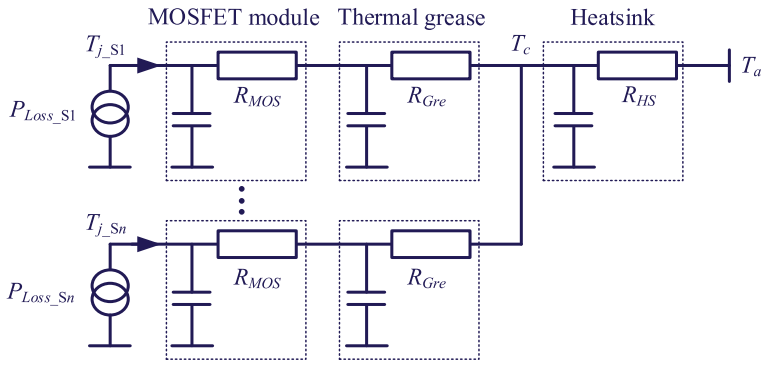


Figure 11: Thermal equivalent model.

3.1.1.3 Structure of MATLAB code for DAB modelling

The modelling of the SiC-based DAB converters is finalized by MATLAB code, whose structure is shown in Figure 12. The main information is summarized as:

(1) The waveforms of the voltages and inductor current can be drawn in MATLAB code, and then, the RMS value of the inductor current and instantaneous voltage and current at switching instants can be determined. In this way, the power losses of the MOSFETs and magnetics can be obtained based on Eqs. (2)-(12);
(2) The junction temperature of the MOSFETs can be obtained based on the thermal equivalent model after the power losses are calculated;
(3) The maximum transferred power of various DAB converters is expressed as

$$\mathrm{P_{max}} = \begin{cases} \dfrac{\mathrm{V_{in}V_{out}}}{32\mathrm{Nf_{sw}L_s}}, \text{half-bridge DAB} \\ \dfrac{\mathrm{V_{in}V_{out}}}{8\mathrm{Nf_{sw}L_s}}, \text{single-phase DAB} \\ \dfrac{\mathrm{V_{in}V_{out}}}{12\mathrm{Nf_{sw}L_s}}, \text{three-phase DAB} \end{cases} \tag{15}$$

Thus, the series inductance can be obtained based on the maximum transferred power, DC voltages, switching frequency, and transformer's turns ratio, i.e.,

$$L_s = \begin{cases} \dfrac{V_{in}V_{out}}{32Nf_{sw}P_{max}}, \textit{half-bridge DAB} \\ \dfrac{V_{in}V_{out}}{8Nf_{sw}P_{max}}, \textit{single-phase DAB} \\ \dfrac{V_{in}V_{out}}{12Nf_{sw}P_{max}}, \textit{three-phase DAB} \end{cases} \tag{16}$$

(4) The paralleled-switch structure is also considered in the DAB converters, as shown in Figure 13. In this structure, several switches are parallel-connected to reduce the current stress on each switch, and the efficiency and reliability of the DAB converters can be improved under certain conditions.

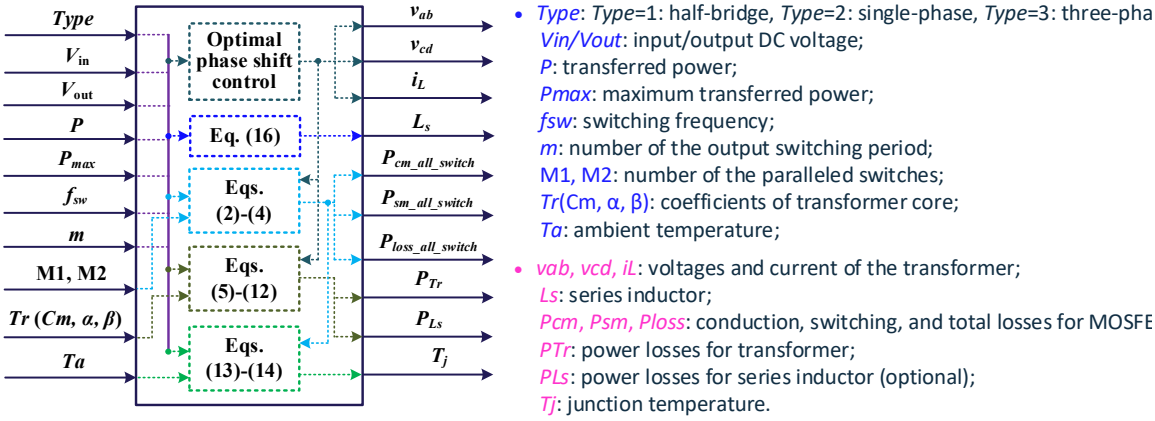


Figure 12: Structure of the MATLAB code for SiC-based DAB converters.

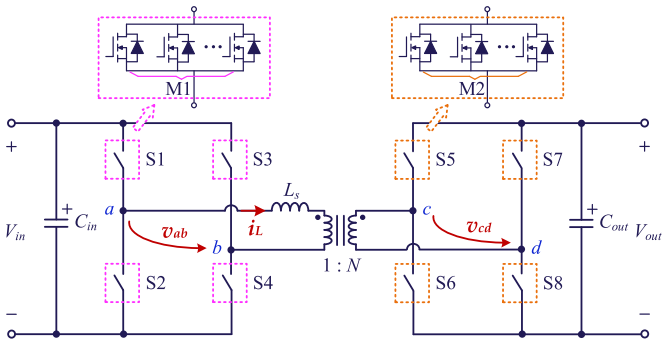
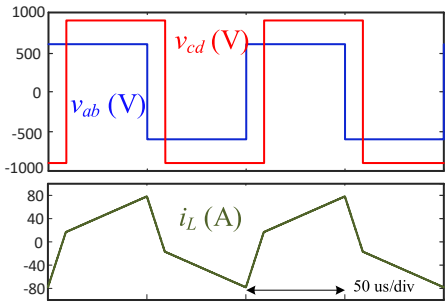


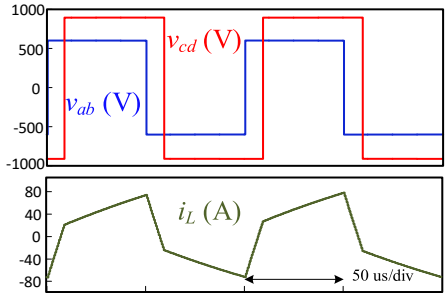
Figure 13: Paralleled-switch structure of the DAB converters.

3.1.1.4 Accuracy verification

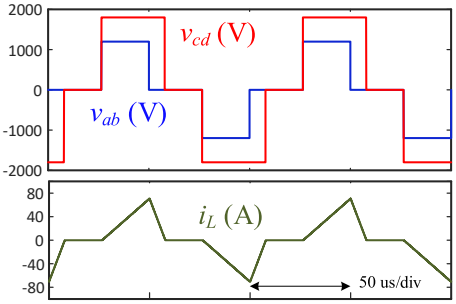
In order to verify the accuracy of the power loss modelling in the MATLAB code, the simulations in PLECS are performed to compare the power losses obtained by PLECS and MATLAB code. Figure 14 shows the waveforms of the voltages and the inductor current from MATLAB code and PLECS under the condition of V_{in} = 1200 V, V_{out} = 1800 V, P = 20 kW. It can be seen from Figure 15 that the waveforms from MATLAB code and PLECS are close. Since the power losses of MOSFETs are determined by the RMS current and instantaneous voltage and current at switching instants, the power losses obtained by MATLAB code and PLECS are close, as shown in Figure 14. Furthermore, Figure 15 shows the comparison of the power losses for all the MOSFETs by MATLAB code and PLECS under various power levels. The loss difference between the two methods is limited during the entire power range, which means the power loss modelling for DAB converters in MATLAB code is accurate, and can be applied for the efficiency, reliability, and cost optimization.



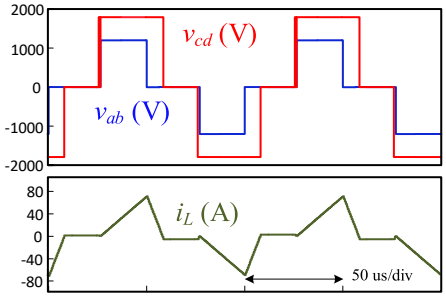
(a) Half-bridge DAB – MATLAB code



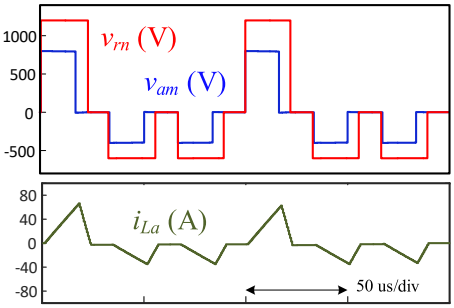
(b) Half-bridge DAB – PLECS



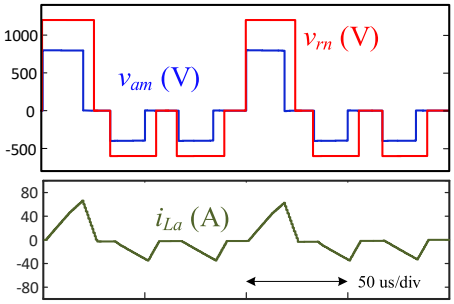
(c) Single-phase DAB – MATLAB code



(d) single-phase DAB – PLECS



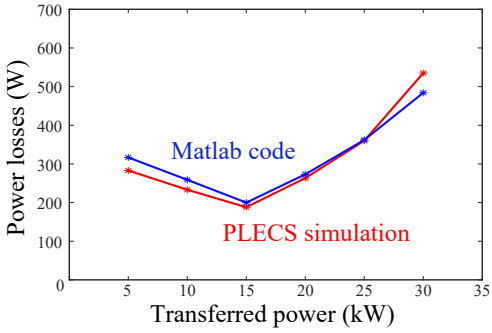
(e) Three-phase DAB – MATLAB code



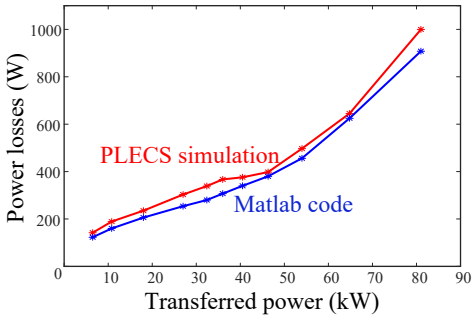
(f) Three-phase DAB – PLECS

Topologies of DAB	Power losses by MATLAB code	Power losses by PLECS
Half-bridge DAB	275 W	263 W
Single-phase DAB	208 W	223 W
Three-phase DAB	230 W	242 W

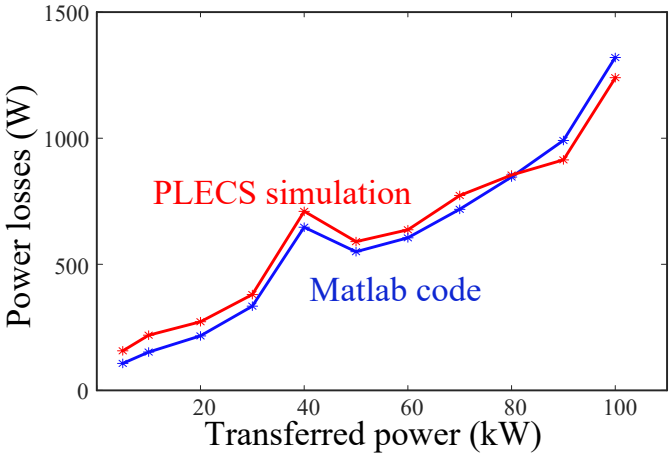
Figure 14: Waveforms of various DAB converters by MATLAB code and PLECS, and corresponding losses.



(a) Half-bridge DAB



(b) Single-phase DAB



(c) Three-phase DAB

Figure 15: Comparison of the power losses by MATLAB code and PLECS under different power levels.

3.1.2 Power loss modelling of MMC converters

3.1.2.1 Overview of MMC converters

MMC back-to-back converters are applied to the wind system for power flow control and frequency conversion, as shown in Figure 16. The main parameters of the MMC converters are shown in Table 9. Two topologies, i.e., half-bridge and full-bridge, are considered in the series-connected MMC cells. For each cell, it can operate in two modes in normal state, i.e., ON mode (inserted mode) and OFF mode (bypass mode), as shown in Table 10. The number of the ON-mode cells will form the output voltage level [10]. Carrier-phase-shifting SPWM (CPS-SPWM) method is used to control the MMC converters in this project [11].

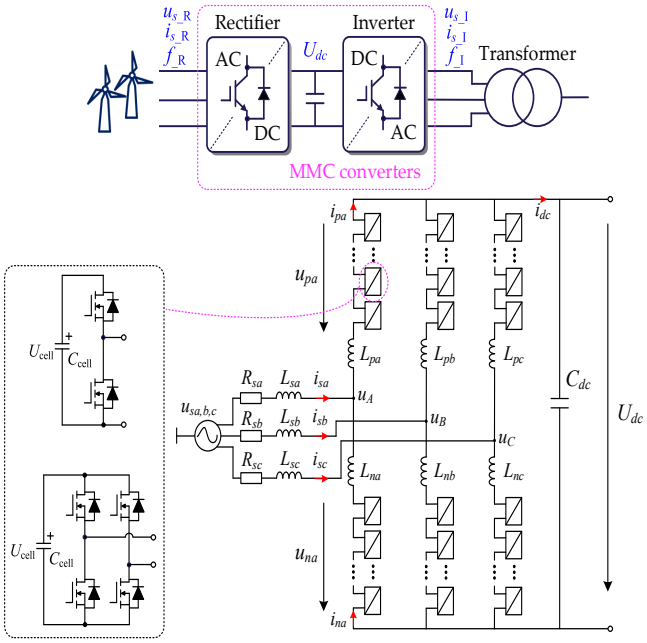
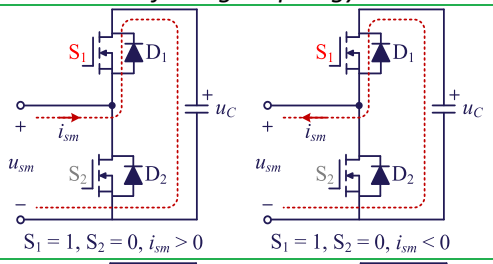
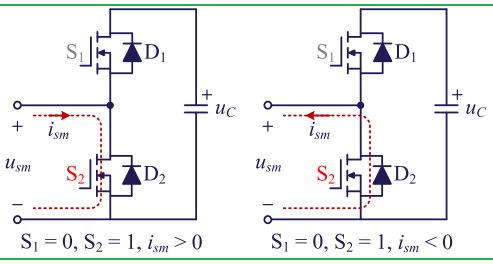
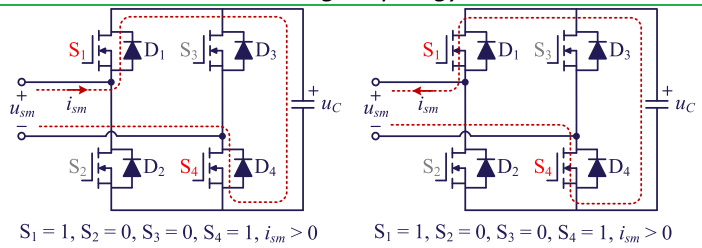
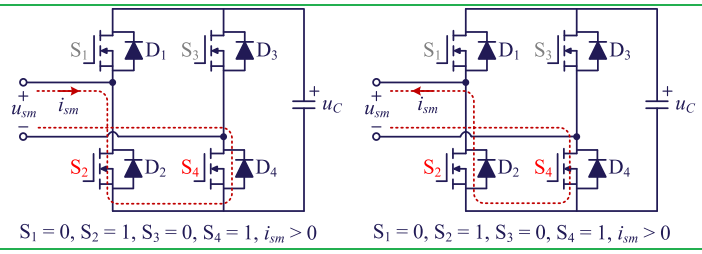


Figure 16: Application of MMC converters.

Table 9. Parameters of MMC converters.

Parameter	Value
AC voltage Us_R & Us_I	6.6 & 6.6 kV
Ac frequency f_R & f_I	25 & 50 Hz
Transferred power P	20 MW
DC voltage Udc	23.3 kV
Cell number Ncell	16
Paralleled number Nparallel	2
Switching frequency fsw	1000 Hz
Arm inductor Lp/Ln	3 mH

Table 10. Operating modes for each cell under half-bridge and full-bridge topologies.

Operating mode	Current flow path	Voltage
Half-bridge topology		
ON mode		$u_{sm} = u_C$
OFF mode		$u_{sm} = 0$
Full-bridge topology		
ON mode		$u_{sm} = u_C$
OFF mode		$u_{sm} = 0$

3.1.2.2 Mathematical model

The equivalent circuit for one phase of MMC converters is shown in Figure 17 [12]. The voltages across all the series-connected cells in upper/lower bridge arm can be expressed as

$$u_{pa} = \frac{U_{dc}}{2} - u_A = n_{pa}U_c \tag{17}$$

$$u_{na} = \frac{U_{dc}}{2} + u_A = n_{na}U_c \tag{18}$$

where n_{pa} and n_{na} are the number of ON-mode cells for the upper and lower bridge arm, respectively, which satisfies $n_{pa} + n_{na} = N_{cell}$. U_c is the capacitor voltage of each cell, which can be expressed as $U_c = U_{dc}/N_{cell}$. Therefore, the voltage u_A can be obtained by

$$u_A = \frac{u_{na} - u_{pa}}{2} \tag{19}$$

Furthermore, the voltage u_A can also be expressed as

$$u_A = u_{sa} - R_{sa} i_{sa} - L_{sa} \frac{di_{sa}}{dt} \tag{20}$$

Combining Eqs. (18) and (19), the phase current i_{sa} can be obtained. The arm currents i_{pa} and i_{na} can be obtained by

$$i_{pa} = \frac{I_{dc}}{3} + \frac{i_{sa}}{2} \tag{21}$$

$$i_{na} = \frac{I_{dc}}{3} - \frac{i_{sa}}{2} \tag{22}$$

With the above equations, the waveforms of the arm currents can be drawn by MATLAB code, and the power losses of MOSFETs and filter inductors can be calculated afterwards.

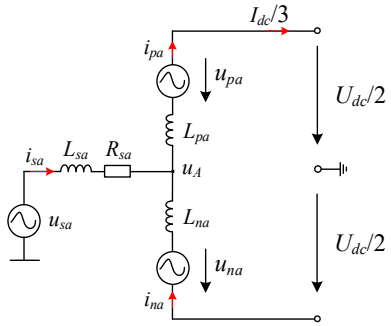


Figure 17: Equivalent circuit for MMC converters.

3.1.2.3 Structure of MATLAB code for MMC modelling

The power loss modelling of MOSFETs and inductors of MMC converters is similar to that of the DAB converters, which can be obtained based on Eqs. (2)-(11), and the thermal modelling can be obtained by Eqs. (13) and (14). Figure 18 illustrates the structure of MATLAB code for MMC back-to-back converters.

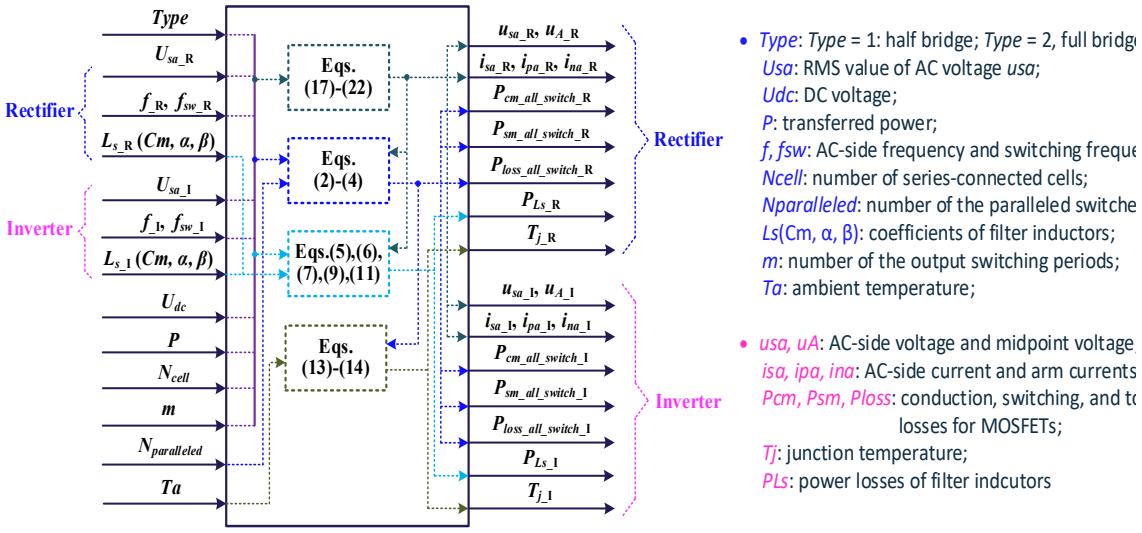
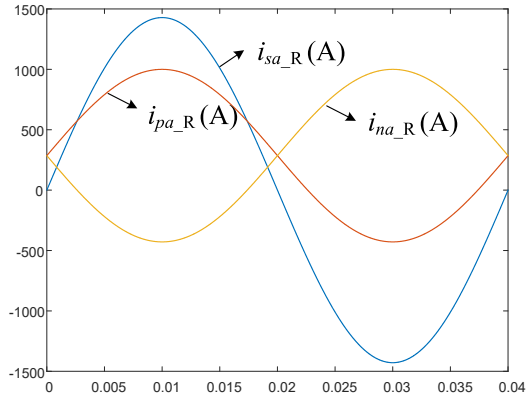
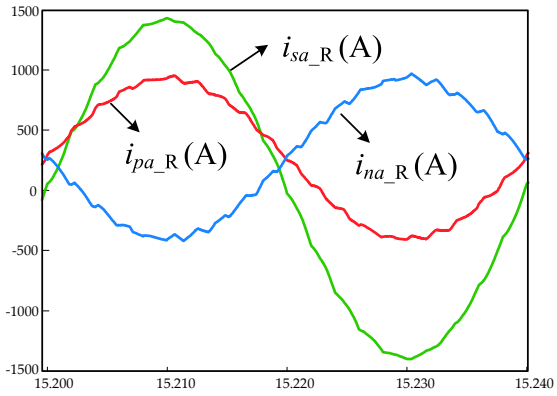


Figure 18: Structure of MATLAB code for MMC back-to-back converters.

3.1.2.4 Accuracy verification

The waveforms of currents from PLECS and MATLAB code for the MMC converters with half-bridge and full-bridge topologies are shown in Figure 19 and Figure 20. It can be seen from Figure 19 and Figure 20 that the current waveforms between PLECS and MATLAB code, and the corresponding power losses are close. Therefore, the accuracy of the power loss modelling for MMC converters from MATLAB code can be verified.





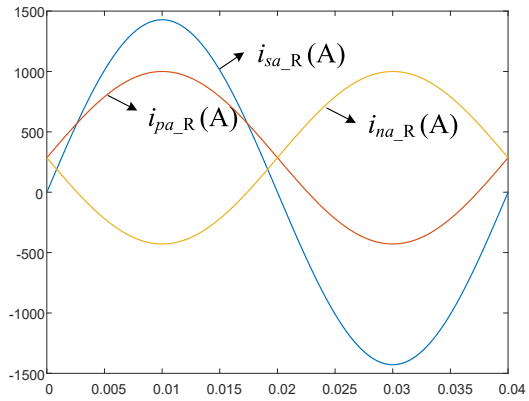
Losses from MATLAB code	*Value*
Conduction losses	*31.6 kW*
Switching losses	*25.9 kW*
Total losses	*57.5 kW*

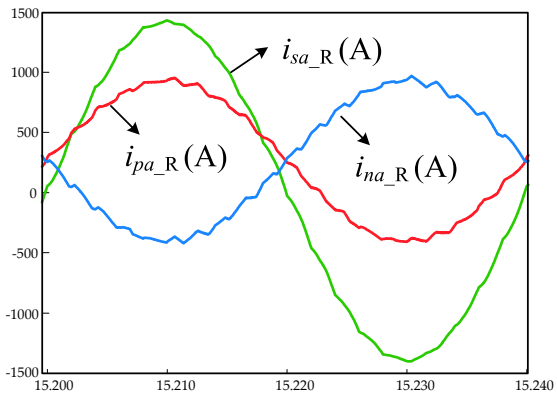
(a)

Losses from PLECS	*Value*
Conduction losses	*30.9 kW*
Switching losses	*24.8 kW*
Total losses	*55.7 kW*

(b)

Figure 19: Waveforms of currents and corresponding losses under P = 20 MW with half-bridge topology from: (a) MATLAB code, and (b) PLECS.





Losses from MATLAB code	*Value*
Conduction losses	*68.7 kW*
Switching losses	*25.6 kW*
Total losses	*94.3 kW*

(a)

Losses from PLECS	*Value*
Conduction losses	*66.5 kW*
Switching losses	*24.6 kW*
Total losses	*91.1 kW*

(b)

Figure 20: Waveforms of currents and corresponding losses under P = 20 MW with full-bridge topology from: (a) MATLAB code, and (b) PLECS.

3.2 COST MODELLING

3.2.1 CAPEX modelling

The framework determines the CAPEX of the system by adding CAPEX of the system cable and the CAPEX of the SiC based converter.

3.2.1.1 System Cable

CAPEX of the system cable is approximated as the total copper price of the cables. In order to find the copper price, copper weight is calculated.

$$V_{cop} = l_{cable} A_{cable} \tag{23}$$

$$W_{cop} = V_{cop} d_{cop} \tag{24}$$

$$CAPEX_{cable} = W_{cop} c_{cop} \tag{25}$$

Cable cross sections are calculated according to DC cable types given in D1.2. of the project. In the deliverable, cable cross-section relationships with the rated current of the cable were provided for onshore and submarine applications.

3.2.1.2 Converter

The converter CAPEX depends on six main components. These components are power switches, MF transformers (medium frequency), capacitors, cabinet-frame, electronics and heatsink-cooling systems. In this project, power switches represent the SiC half-bridge modules provided by a project partner.

In the converter design, the capacitor is selected as EPCOS/TDK B25690A2187K003. Cost of this product is given as 80 € in [13]. Depending on the selected topology of the submodules and the number of submodules, different number of capacitors are necessary in the converter.

$$CAPEX_{cap} = n_{cap} c_{cap} \tag{26}$$

Other components of the converter CAPEX are MF transformer, cabinet-frame, electronics and cooling system-heatsink. CAPEX of these components is proportional with the power level of the converter. Cost of these components depends on the literature [14].

$$CAPEX_{transformer} = CAPEX_{reftrans} \left(\frac{P_{conv}}{P_{ref}} \right) \tag{27}$$

$$CAPEX_{cabinet-frame} = CAPEX_{refcabinet-frame} \left(\frac{P_{conv}}{P_{ref}} \right) \tag{28}$$

$$CAPEX_{electronics} = CAPEX_{refelectronics} \left(\frac{P_{conv}}{P_{ref}} \right) \tag{29}$$

$$CAPEX_{coolingsystem-heatsinks} = CAPEX_{refcoolingsystem-heatsink} \left(\frac{P_{conv}}{P_{ref}} \right) \tag{30}$$

Total capex is obtained with summation of all CAPEX components.

$$CAPEX_{converter} = CAPEX_{transformer} + CAPEX_{powerswitch} + CAPEX_{cap} + CAPEX_{cabinet-frame} + CAPEX_{electronics} + CAPEX_{coolingsystem-heatsink} \quad (31)$$

$$CAPEX = CAPEX_{cable} + CAPEX_{converter} \quad (32)$$

3.2.2 OPEX modelling

Economic analysis of a MW scale power converter (LLC-HVDC) is investigated in [15]. Three components are included as operational cost, total lost energy price, maintenance-operation and disposal costs.

The total lost energy is calculated by summing all the lost energy for 24 hours. Then, it is multiplied by 365 to extend the calculation for a year. Lastly, the total lost energy is multiplied by the average energy price (0.10 €/kWh) to obtain the total cost of lost energy.

$$E_{lostenergy} = E_{switchingloss} + E_{conductionloss} + E_{transformerloss} + E_{inductorloss} \quad (33)$$

$$OPEX_{lostenergy} = E_{lostenergy}\, c_{electrical-energy} \quad (34)$$

The annual maintenance and operation costs of a converter are calculated as 2% of the total converter CAPEX in [15]. Therefore, the total maintenance and operation costs are calculated by multiplying this number with total years of service. Total years of service (n_{years}) is considered as 30 years in this deliverable.

$$OPEX_{maintenance-operation} = CAPEX_{converter} n_{years} 0.02 \quad (35)$$

The last item of the OPEX is the disposal cost [13]. This cost includes the remanent and recycling cost of the converter. It is considered as -%5 of the total converter CAPEX and it is realized at the end of the converter lifecycle.

The summation of these three OPEX components provides the total OPEX

$$OPEX = OPEX_{lostenergy} + OPEX_{maintenance-operation} + OPEX_{disposal} \quad (36)$$

The Total Cost of Ownership (TCO) for the converter is calculated with the summation of CAPEX and OPEX.

$$TCO_{converter} = CAPEX_{converter} + OPEX_{converter} \quad (37)$$

$$TCO_{system} = TCO_{converter} + TCO_{systemcable}$$

3.3 RELIABILITY MODELLING

The objective of this function is to determine the lifetime of an SST or an MMC. The lifetime is calculated through a reliability assessment. The reliability is defined as the probability of a device fully operating after a certain amount of time. In this work, reliability is targeted as 90% for a converter. Lifetime is calculated as the amount of time after which the converter will be working with 90% chance.

Power semiconductor devices (PSD) of a converter are the least reliable components; therefore, reliability of the converter depends on PSDs. In this work, constant failure rate λ is used to model the reliability of a PSD. The expression for reliability is given in Eq. (38). Note that, the switch reliability is denoted with $R_{switch}(t)$ where t denotes time.

$$R_{switch}(t) = e^{-\lambda t} \tag{38}$$

Depending on the type of the submodule topology, different number of PSDs are used in one submodule. Since the probability of failure for different PSDs are independent from each other, the reliability of a submodule can be expressed as presented in Eq. (39). In this equation, $R_{SM}(t)$ represents the submodule reliability at time t while n_{switch} represents the total number of switches in one submodule.

$$R_{SM}(t) = R_{switch}(t)^{n_{switch}} = e^{-\lambda t n_{switch}} \tag{39}$$

The last step is to find the converter level reliability. Since the failure rate of submodules is independent of each other, the reliability of a converter can be expressed as in Eq. (40). In this equation $R_{conv}(t)$ represents the converter reliability at time t while n_{sm} represents the number of submodules in the converter.

$$R_{conv}(t) = R_{SM}(t)^{n_{sm}} = e^{-\lambda t n_{switch} n_{sm}} \tag{40}$$

In this expression, if the converter reliability is considered as 0.9. Variable *t* can be determined as lifetime.

The reliability of the PSD is affected by the temperature and the switch voltage. The temperature factor is shown in Eq. (41). In this equation, π_t represents the temperature factor, K represents the temperature coefficient, T_{j1} represents the junction temperature of the switch and T_{j2} represents the reference junction temperature.

$$\pi_t = e^{K\left(\frac{1}{T_{j1}} - \frac{1}{T_{j2}}\right)} \tag{41}$$

In a multilevel SST converter, the reliability is low due to a high number of components. In order to increase the reliability of a converter, redundant submodules are added to increase the reliability. These submodules are turned off and disconnected from the converter in normal operation. If a failure occurs in one of the main submodules, a redundant submodule will be turned on and replace the failed submodule. The reliability of the converter with redundant SMs is shown in Eq. (42). In this equation, N represents the total number of submodules, n represents the number of main submodules and C represents the combination operator.

$$R_{conv}(N,t) = \sum_{i=n}^{N} C_i^N R_{SM}(N,t)^i \left(1 - R_{SM}(N,t)\right)^{N-i} \tag{42}$$

4 PERFORMANCE OF THE SELECTED PE SYSTEM ARCHITECTURES

The optimisation framework results are presented in this section. Three distinct sets of results are provided for three different use cases.

The initial results of the optimisation consist of Pareto solution sets for each of the three use cases. These sets are visually represented in Figure 21, Figure 24 and Figure 27. On the x-axis of these figures, the expected lifetime of a single converter is shown, while the y-axis represents the CAPEX of the combined converter and cable system. The CAPEX is normalized to set the maximum CAPEX equal to one in each use case. Lastly, the efficiency of each solution is indicated using a colour bar on each figure.

The solutions are evaluated in terms of CAPEX, lifetime and efficiency. For each use case, solutions with the maximum lifetime, maximum efficiency and minimum CAPEX are identified and marked on the Pareto solution sets. These solutions are referred to as intermediate solutions.

The variables utilized to reach the intermediate solutions are described in Table 11, Table 15 and Table 19 while the corresponding results are presented in Table 12, Table 16 and Table 20. The breakdown of power losses for the intermediate solutions are illustrated in Figure 22, Figure 25 and Figure 28.

In order to determine the best solution for each use case, a weight function is utilized. The purpose of the weight function is to keep the TCO of the system low. The expression of the weight function is shown in Eq. (43). In this expression S represents the selection criteria, $f_{efficiency}$ represents the efficiency objective function, $f_{lifetime}$ represents the lifetime objective function and f_{cost} represents the cost objective function which is the CAPEX.

$$S = 45\%\, f_{efficiency} + 10\%\, f_{lifetime} - 45\%\, f_{cost} \tag{43}$$

The variables used to obtain the best solutions are provided in Table 13, Table 17 and Table 21, with corresponding results are given in Table 14, Table 18 and Table 22. Furthermore, the lost breakdowns for each best case are shown in Figure 23, Figure 26 and Figure 29.

4.1 OPTIMIZATION RESULTS FOR THE FIRST USE CASE (PV-SST)

4.1.1 Pareto front solutions

The set of Pareto solutions for the PV-SST use case is represented in Figure 21.

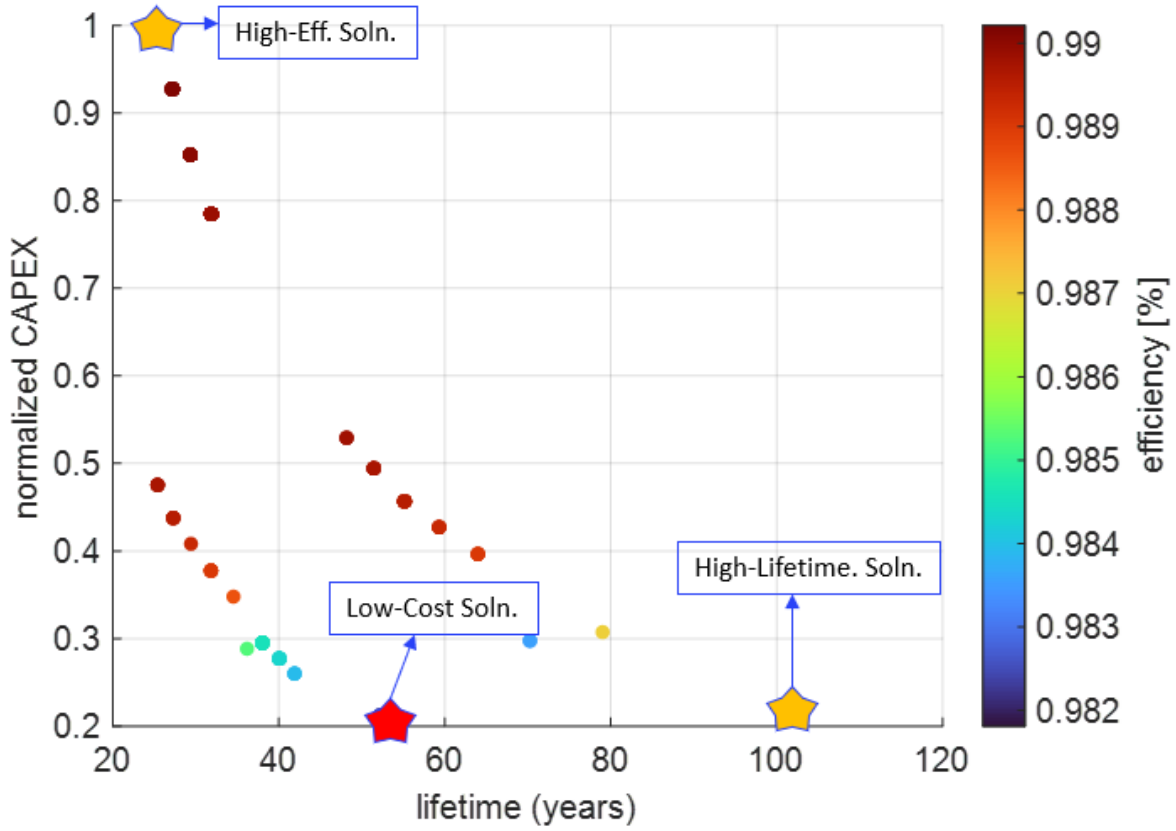


Figure 21: Pareto Optimal Solutions for PV-SST Use Case

4.1.2 Intermediate Solutions

Several observations about the intermediate solutions are listed below:

- The high-efficiency solution is obtained by employing two parallel switches instead of one and using the three phase DAB topology instead of using the half bridge topology. This is because the three phase DAB has the highest efficiency within the three topologies and using parallel switches effectively reduces the on-state resistance.
- The low-cost solution is obtained by using half bridge topology with low number of submodules. However, this solution is limited by high temperature and low efficiency.
- The high-lifetime solution employs a half bridge topology and 2 redundant submodules. Since the half bridge topology has fewer switches than the three phase DAB, it provides a higher reliability and higher lifetime.
- The loss breakdowns suggest that the switching losses are dominant to other losses.

Table 11: Intermediate Solution Variables for PV-SST Use Case

Selected Variables			
	High-Efficiency Soln.	*Low-Cost Soln.*	*High-Lifetime Soln.*
Medium voltage level	*41 kV*	*38 kV*	*41 kV*
Redundant submodule number	*2*	*1*	*2*
SM topology	*Three-phase DAB*	*Half-bridge topology*	*Half-bridge topology*
Switching frequency	*12 kHz*	*12 kHz*	*12 kHz*
No of parallel switches	*2*	*1*	*1*
Max switch voltage	*1.8 kV*	*1.8 kV*	*1.8 kV*

Table 12: Intermediate Solution Results for PV-SST Use Case

Results			
	High-Efficiency Soln.	*Low-Cost Soln.*	*High-Lifetime Soln.*
Efficiency	*99.02 %*	*98.18 %*	*98.25 %*
Normalized CAPEX	*1.00*	*0.20*	*0.22*
Lifetime	*25 years*	*54 years*	*101 years*
Submodule power rating	*110 kW*	*120 kW*	*110 kW*
Main SM No	*23*	*21*	*23*
Max T_J	*40 °C*	*145 °C*	*128 °C*
Average T_J	*32 °C*	*51 °C*	*48 °C*
Max transformer current	*97 A*	*317 A*	*290 A*

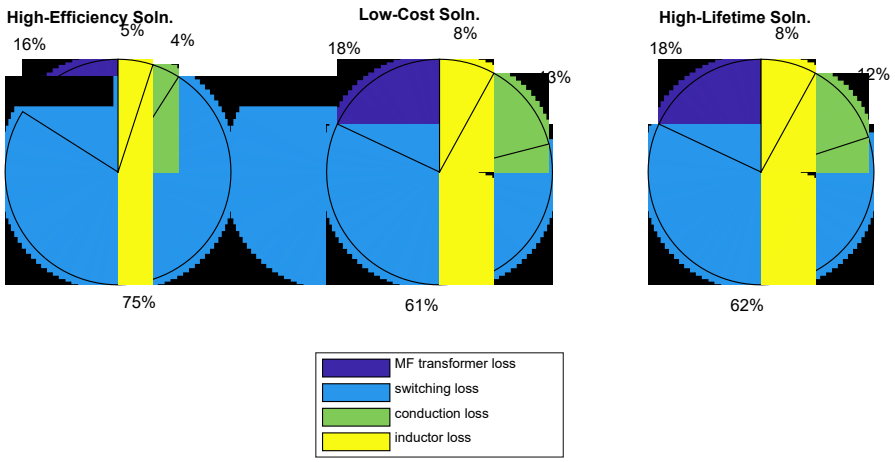


Figure 22: Electrical Losses Breakdown of the Intermediate Solutions

4.1.3 Best Solution

The low-cost solution is identified as the best solution according to the weight function. Several observations about the best solution are listed below.

- Main submodule number of the converter is selected as 21. Less number of submodules cannot be used since the junction temperature is at the limit. On the other hand, increasing the number of submodules increases the cost.

- Redundant submodule number is selected as 1. Increasing the number of redundant submodules increases the lifetime; however, the lifetime is already high. On the other hand, using zero redundant submodules reduces the lifetime to less than 10 years which is not desired.
- The half bridge topology is selected instead of the three phase DAB topology because of the low switch number which reduces the CAPEX significantly.
- Having more than one parallel switch increases the efficiency slightly; however, it causes CAPEX to increase dramatically. Therefore, a single parallel switch is preferred.
- Maximum switch voltage is kept at 1.8 kV since increasing this value decreases the lifetime dramatically.

Table 13: Best Solution Variables for PV-SST Use Case

Selected Variables	
Medium voltage level	*38 kV*
Redundant submodule number	*1*
SM topology	*Half-bridge topology*
Switching frequency	*12 kHz*
No of parallel switches	*1*
Max switch voltage	*1.8 kV*

Table 14: Best Solution Results for PV-SST Use Case

Results	
Efficiency	*98.18 %*
CAPEX	*0.20*
Lifetime	*54 years*
Submodule power rating	*120 kW*
Main SM No	*21*
Max T_J	*145 °C*
Average T_J	*51 °C*
Max transformer current	*317 A*

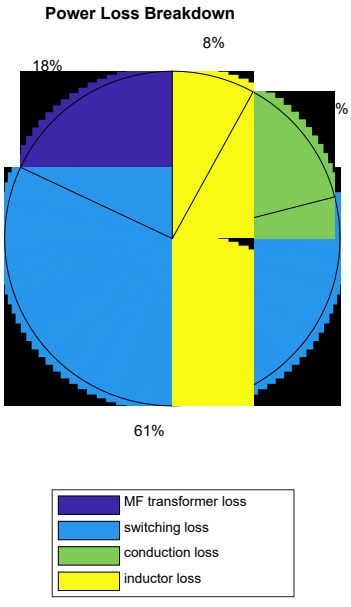


Figure 23: Electrical Losses Breakdown of the Best Solution

4.2 OPTIMISATION RESULTS FOR THE SECOND USE CASE (WIND-MMC)

4.2.1 Pareto front solutions

The set of Pareto solutions for the Wind-MMC use case is represented in Figure 24.

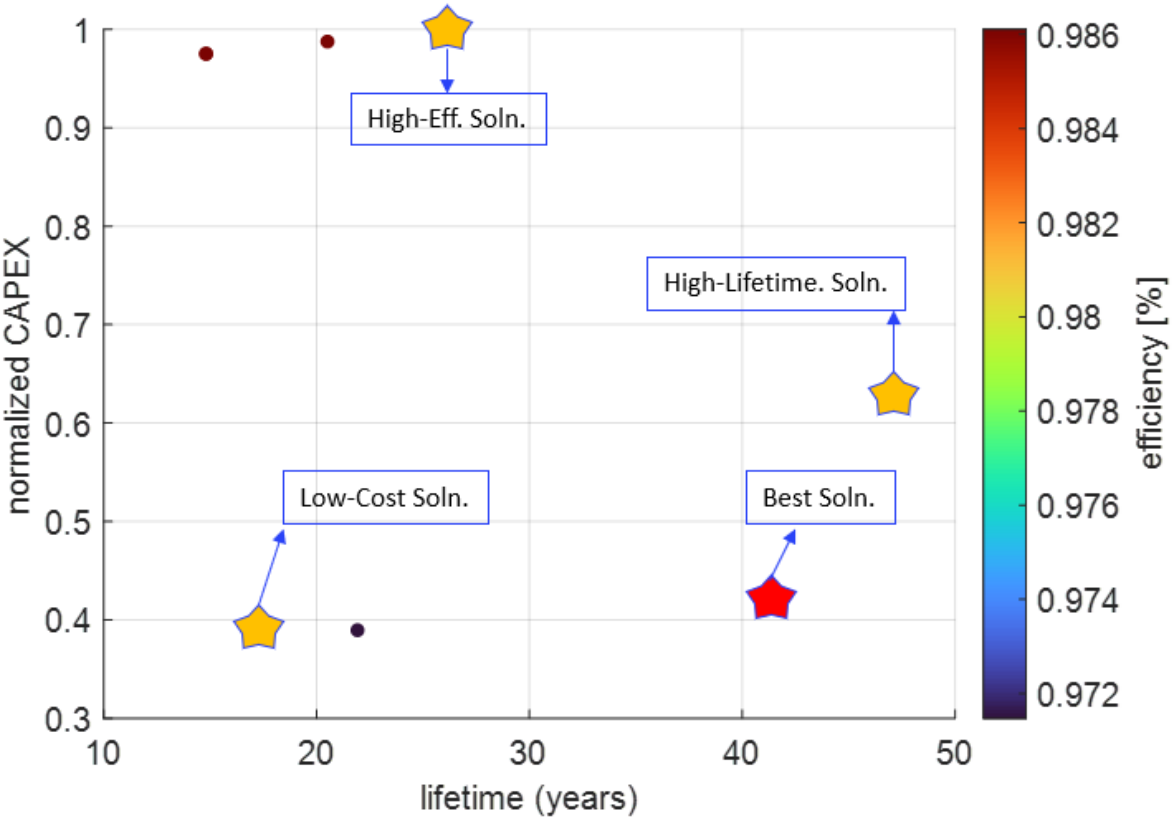


Figure 24: Pareto Optimal Solutions for Wind-MMC Use Case

4.2.2 Intermediate Solutions

Several observations about the intermediate solutions are listed below:

- All intermediate solutions adopt half bridge topology due to its lower cost.
- The high-efficiency solution utilizes maximum number of parallel switches to increase the efficiency.
- The low-cost solution utilizes lowest number of switches to operate the system. However, the maximum current on the switch is above the current limit of the SiC module; therefore, parallel switches must be used in the MMC design.
- The high-lifetime solution has lower switch number; hence, its complexity is lower than other cases.

Table 15: Intermediate Solution Variables for Wind MMC Use Case

Selected Variables			
	High-Efficiency Soln.	*Low-Cost Soln.*	*High-Lifetime Soln.*
Switching frequency	*800 Hz*	*800 Hz*	*800 Hz*
No of parallel switch	*3*	*1*	*3*
Number of cells in one arm	*12*	*13*	*7*
Cell Type	*Half-bridge*	*Half-bridge*	*Half-bridge*
Redundant cell number	*5*	*4*	*5*
DC-link voltage	*21.6 kV*	*23.4 kV*	*12.6 kV*

Table 16: Intermediate Solution Results for Wind MMC Use Case

Results			
	High Efficiency Soln.	*Low-Cost Soln.*	*High Lifetime Soln.*
Efficiency	*98.61 %*	*97.15 %*	*98.37 %*
CAPEX	*1.00*	*0.39*	*0.63*
Lifetime	*26 years*	*17 years*	*47 years*
Rectifier maximum junc. temp	*62 °C*	*149 °C*	*59 °C*
Inverter maximum junc. temp	*62 °C*	*147 °C*	*58 °C*
Rectifier average junc. temp	*59 °C*	*136 °C*	*56 °C*
Inverter average junc. temp	*58 °C*	*131 °C*	*54 °C*
Maximum arm current	*1023 A*	*999 A*	*1243 A*
Maximum switch current	*341 A*	*999 A*	*414 A*

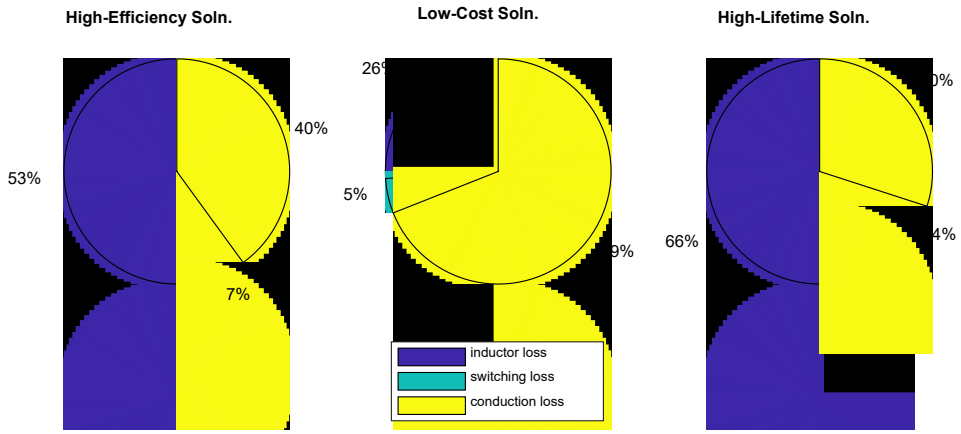


Figure 25: Electrical Losses Breakdown of the Intermediate Solutions

4.2.3 Best Solution

The best solution is selected as follows:

- The best result is obtained when the DC-link voltage is relatively low. This is because the switch cost is lower with a lower number of cells in one arm.
- The cell type is selected as half bridge because a full bridge cell increases the number of switches which leads to a higher CAPEX.
- Moreover, increasing the parallel connected switch number did not create a benefit because, although it increases the efficiency, it also increases the initial cost.

Table 17: Best Solution Variables for Wind-MMC Use Case

Selected Variables	
Switching frequency	*800 Hz*
No of parallel switch	*2*
Number of cells in one arm	*7*
Cell Type	*Half bridge*
Redundant cell number	*4*
DC-link voltage	*12.6 kV*

Table 18: Best Solution Results for Wind MMC Use Case

Results	
Efficiency	*98.10 %*
CAPEX	*0.42*
Lifetime	*41 years*
Rectifier maximum junc. temp	*76 °C*
Inverter maximum junc. temp	*74 °C*
Rectifier average junc. temp	*71 °C*
Inverter average junc. temp	*69 °C*
Maximum arm current	*1243 A*
Maximum switch current	*622 A*

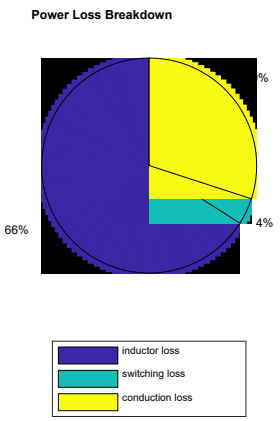


Figure 26: Electrical Losses Breakdown of the Best Solution

4.3 OPTIMISATION RESULTS FOR THE THIRD USE CASE (WIND-SST)

4.3.1 Pareto front solutions

The set of Pareto solutions for the Wind-MMC use case is represented in Figure 27.

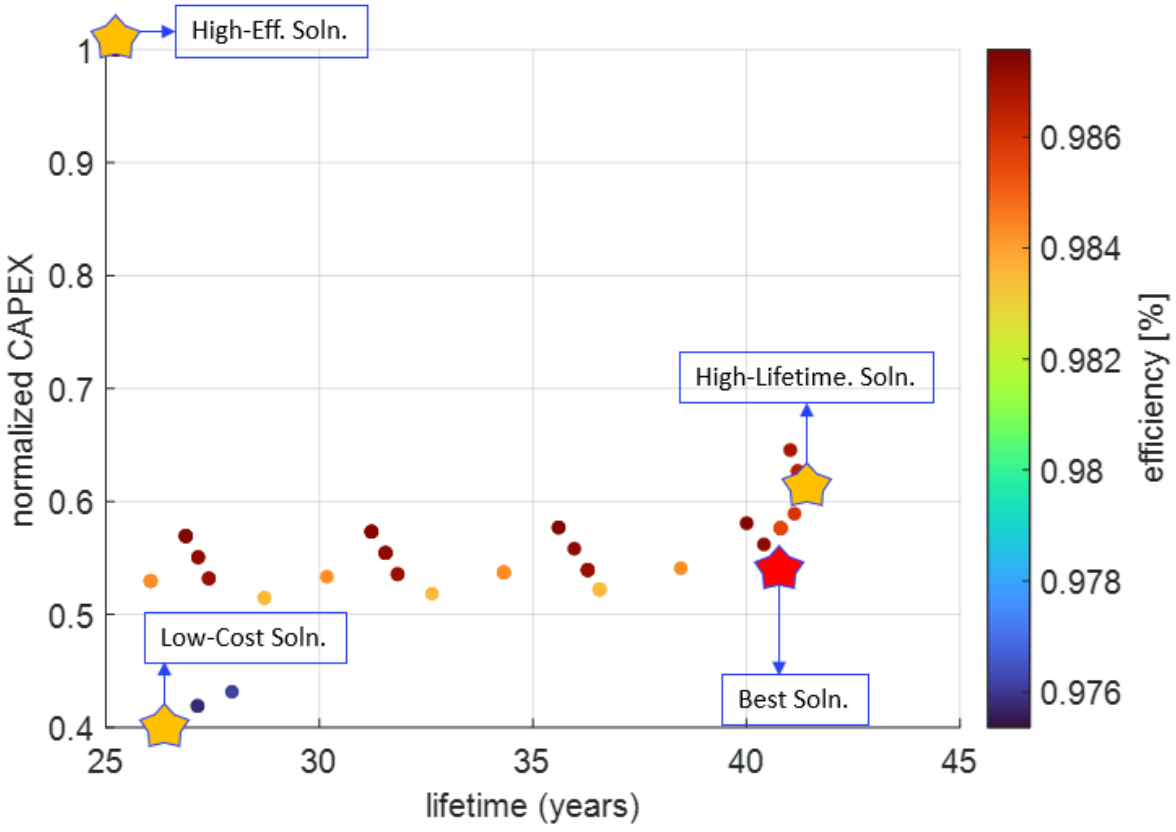


Figure 27: Pareto Optimal Solutions for Wind-SST Use Case

4.3.2 Intermediate Solutions

Several observations about the intermediate solutions are listed below:

- All the intermediate solutions are obtained with high voltage due to reduced cable cost at these voltage values. However, their insulation feasibility should be evaluated in the design.
- Redundant submodule number is selected as 10 to keep the lifetime of the converter more than 25 years. Solutions with lower lifetime are omitted.
- It is observed that adding parallel switch to the system increases the efficiency slightly; however, it increases the cost dramatically.

Table 19: Intermediate Solution Variables for Wind-SST Use case

Selected Variables			
	High-Efficiency Soln.	*Low-Cost Soln.*	*High-Lifetime Soln.*
Medium voltage level	*162 kV*	*180 kV*	*153 kV*
Redundant submodule number	*10*	*10*	*10*
SM topology	*Three-phase DAB*	*Single-phase DAB*	*Three-phase DAB*
Switching frequency	*12 kHz*	*12 kHz*	*12 kHz*
No of parallel switches	*2*	*1*	*1*
Max switch voltage	*1.8 kV*	*1.8 kV*	*1.8 kV*

Table 20: Intermediate Solution Results for Wind-SST Use Case

Results			
	High-Efficiency Soln.	*Low-Cost Soln.*	*High-Lifetime Soln.*
Efficiency	*98.76 %*	*97.54 %*	*98.63 %*
CAPEX	*1.00*	*0.41*	*0.61*
Lifetime	*25 years*	*26 years*	*41 years*
Submodule power rating	*28 kW*	*25 kW*	*29 kW*
Main SM No	*90*	*100*	*85*
Max T_J	*57 °C*	*136 °C*	*72 °C*
Average T_J	*54 °C*	*111 °C*	*68 °C*
Max transformer current	*165 A*	*222 A*	*174 A*

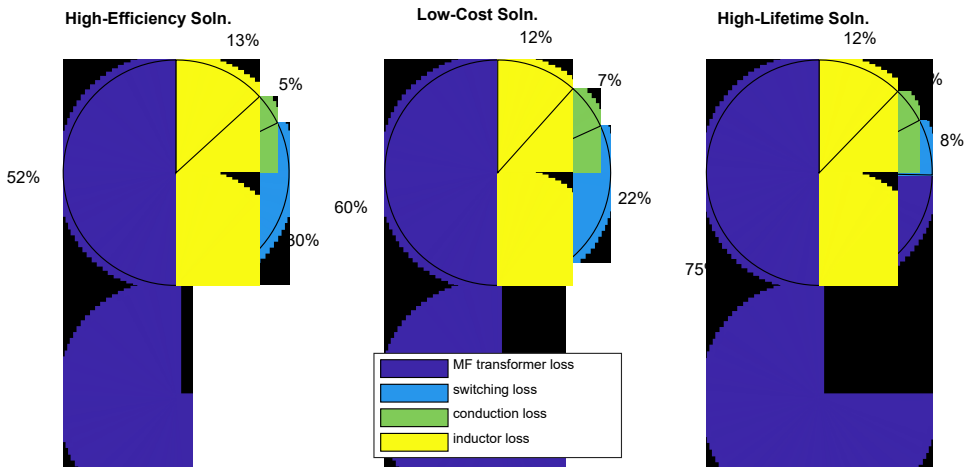


Figure 28: Electrical Losses Breakdown of the Intermediate Solutions

4.3.3 Best Solution

- The best solution is obtained with 100 main submodules. Increasing the submodule number increases the converter cost. On the other hand, reducing the submodule number increases the system cable cost.
- Similar to PV-SST use case, using more than 1 parallel switch or increasing the maximum switch voltage reduces the lifetime dramatically and; therefore, not beneficial.
- Reducing the redundant submodule number reduces the lifetime of the converter to less than 25 years.

Table 21: Best Solution Variables for Wind-SST Use Case

Selected Variables	
Medium voltage level	*180 kV*
Redundant submodule number	*10*
SM topology	*Three-phase DAB*
Switching frequency	*12 kHz*
No of parallel switch	*1*
Max switch voltage	*1.8 kV*

Table 22: Best Solution Results for Wind-SST Use Case

Results	
Efficiency	*98.70 %*
CAPEX	*0.54*
Lifetime	*41 years*
Submodule power rating	*25 kW*
Main SM No	*100*
Max T_J	*64 °C*
Average T_J	*60 °C*
Max transformer current	*148 A*

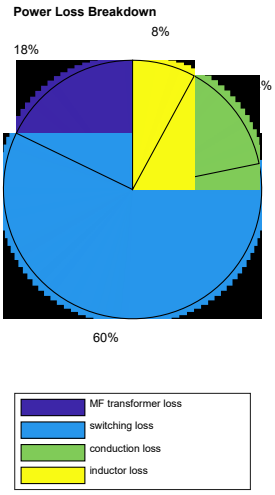


Figure 29: Electrical Losses Breakdowns of the Best Solution

5 CONCLUSION

This deliverable presents the methodology and results of the optimal energy converter architecture selection for MMCs and SSTs within the three use cases of the SiC4GRID project. To fulfil this objective, an optimisation framework has been designed and implemented. The optimisation framework operates to find the architecture with the maximum efficiency, maximum lifetime and minimum cost.

The optimisation framework includes electro-thermal modelling, cost modelling and reliability modelling to determine the efficiency, cost and lifetime of the converter. The electro-thermal model utilizes switch data, circuit topology and thermal design to obtain different types of electrical losses and the semiconductors junction temperature. The cost model depends on the converter cost and the system cable cost to determine the CAPEX and depends on electrical energy and maintenance costs to determine the OPEX. Lastly, the lifetime of the converter is defined as the period during which its reliability remains above 90%. Therefore, the lifetime model depends on the reliability and failure rate of the SiC switches. Through these three primary models, the optimisation framework is proficient in characterizing the objective functions for optimisation.

The optimisation results indicate that the optimal topology depends on the use case, with efficiencies consistently exceeding 98% across all use cases. Furthermore, it is possible to keep the lifetime of the converter above 25 years by using redundant submodules. The cost comparison with the Silicon technology is not included in the deliverable since the two technologies have different types of converters and transformers, making the comparison less relevant. Finally, it is important to note that the results in the deliverable are based on the low- to medium-fidelity modelling developed on the project. In the following activities of the SiC4Grid project, higher-fidelity models will be implemented.

Overall, a comprehensive optimisation tool has been developed for a proper converter architecture design and selection considering different use cases, system constraints and objective weights.

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